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NSLS-II BxB BPM and Hypervisor VM EPICS Interface



U.S. DEPARTMENT OF



Kiman Ha, on behalf of the DSSI I&C and Accelerator D&I

Outline

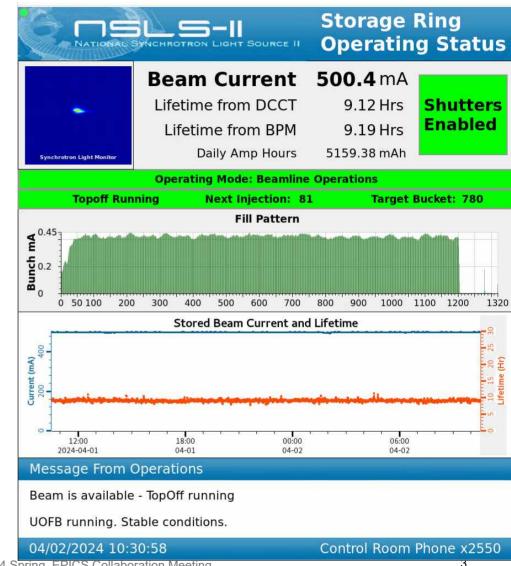
NSLS-II quick status
BxB BPM update status
Hypervisor VM-based IOC and Clients
BxB BPM beam test examples
Summary

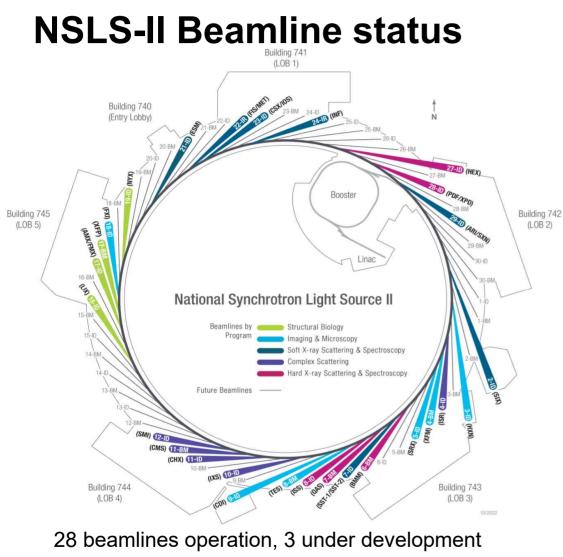
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NSLS-II Main parameters for SR

NSLS-II High Brightness	
Ring energy (GeV)	3
Ring current (mA)	500
Ring circumference (m)	792
Number of DBA Cells	30
Number of 9.3 m straights	15
Number of 6.6 m straights	15
Vertical emittance (nm-rad)	0.008
Horizontal emittance (nm-rad)	0.55
RMS energy spread (%)	0.1
RMS pulse length (ps)	15-30
Time between bunches (ns)	2
Revolution period (us)	2.64
RF frequency (MHz)	500
Number of RF buckets	1320
Number of bunches	1056
Average bunch current (mA)	0.47
Average bunch charge (nC)	1.25

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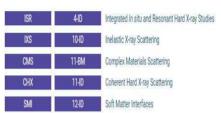




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NSLS-II beamline diagram based on current funding assumptions

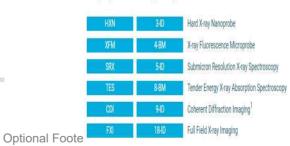
Complex Scattering Program



Hard X-Ray Scattering & Spectroscopy Program

BMM	6-BM	Beamline for Materials Measurement
QAS	7-BM	Quick x-ray Absorption and Scattering
ISS	8-ID	Inner-Shell Spectroscopy
HEX	27-ID	High Energy Engineering X-ray Scattering
PDF	28-ID-1	Pair Distribution Function
XPD	28-ID-2	X-ray Powder Diffraction

Imaging & Microscopy Program



Soft X-Ray Scattering & Spectroscopy Program

SIX	2-ID	Soft Inelastic X-ray Scattering
SST1	7-ID-1	Spectroscopy Soft and Tender
SST2	7-ID-2	Spectroscopy Soft and Tender 2
ESM	21-ID	Electron Spectro-Microscopy
FIS	22-IR-1	Frontier Synchrotron Infrared Spectroscopy
MET	22-IR-2	Magnetospectroscopy, Ellipsometry and Time-Resolved Optical Spectroscopies -> IR spectroscopy, microspectroscopy and nanospectroscopy
CSX	23-ID-1	Coherent Soft X-ray Scattering beamline
IOS	23-ID-2	In situ and Operando Soft X-ray Spectroscopy
SXN	29-ID-1	Soft X-ray Nanoprobe ¹
ARI	29-ID-2	NanoARPES and NanoRIXS ¹

Structural Biology Program



Propose of the new development

- □ Facility Improvement Project (Selected in 2023)
 - D Physics: Model-independent lattice characterization (needed 2 dedicated BxB bpm)
- Engineering: Adopting the new generation RFSoC FPGA technology for the accelerator system
- Provides a new diagnostics tool for unique applications
 - □ BxB transverse beam position measurement
 - □ Calibrate beam oscillation
 - Bunch charge measurement
 - Injection transient measurement
 - Coupled bunch instability measurement
 - □ Beam dump analysis

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RF BPM vs. BxB BPM

- ❑ Analog LPF&BPF (500 MHz +/-5M)
- ❑ ADC sub-sampling ~117 MHz (RF=500 MHz)
- Digital Down Conversion
 - I/Q demodulation
- Decimation low pass filter(FIR, CIC, Averaging) for TBT, FA, SA
- Narrow band high resolution (sub um/nm)
- □ Slow/Fast orbit feedback, beam diagnostics, COB monitoring...

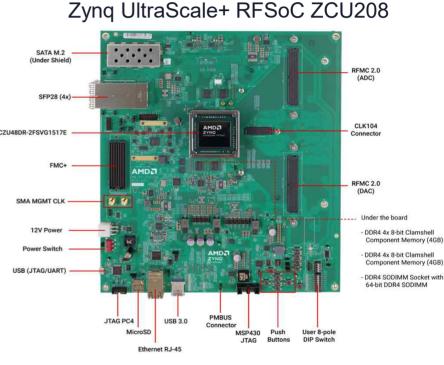
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- Analog LPF > 1GHz (No BPF)
- ADC direct over-sampling 0.5G ~ 5 GHz (RF=500 MHz)
- Negative/Positive peak or averaging bunch amplitude processing(No I/Q)
- Direct conversion bunch amplitude to BxB position
- Decimation low pass filter(FIR, CIC, Averaging) for TBT, SA
- Wide band(~1 GHz), include Image signals
- Dedicated beam performance analysis

BxB BPM hardware key features

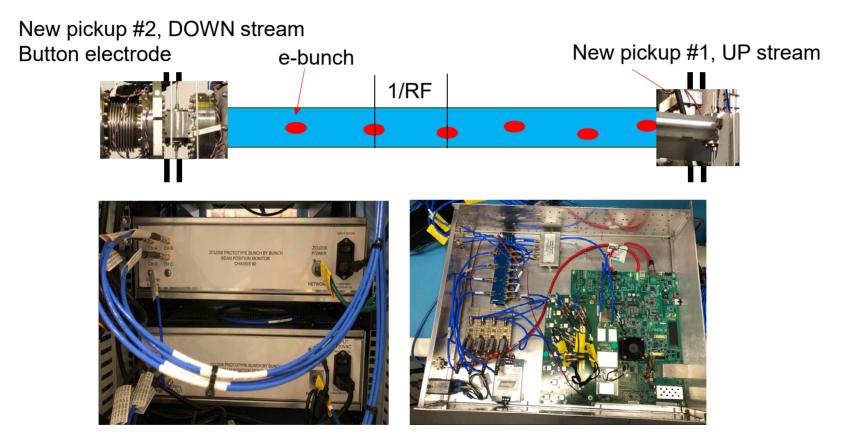
- Quad-core Arm® Cortex®-A53 processing subsystem
- 14-bit 8-channel ADC, max 5 Gsps (configure 4.9968 GHz 4 channels, oversampled BPM button processing, one channel used for RF reference processing)
- 14-bit 8-channel DAĆ, max 7 Gsps (1 channel used for ADC calibration ton generation, xczu480R-2F5VG1517E programable frequency, and gain controls)
- AFE amplifier gain 19 dB (1 stage amplifier)
- Low pass filter 2 GHz and 1 GHz @ 3 dB
- RF input switches for ADC calibration (selectable button signal or calibration tone signal)
- 2-stage PLL for generating ADC clock and FPGA processing clock
- 1 Gbps Ethernet for control system interface
- 2.5 Gbps Event Receiver for timing interface

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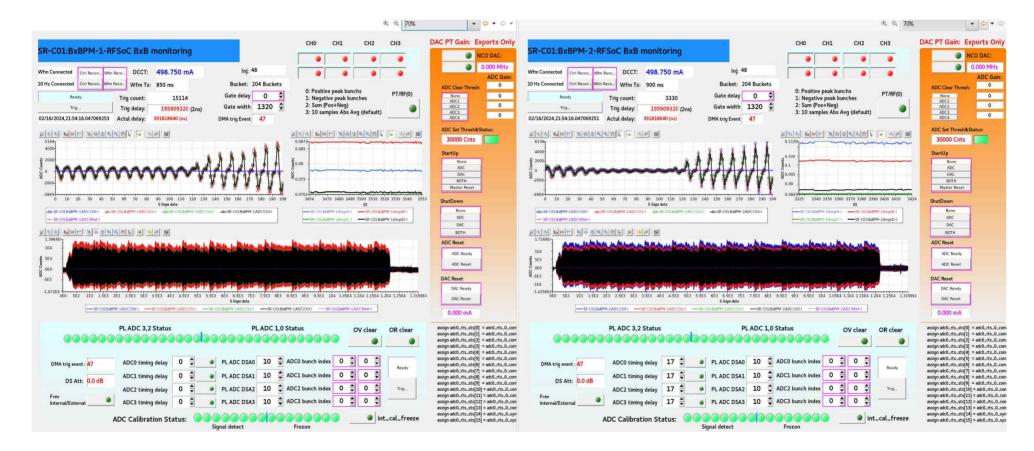
Source: AMD

Location: C01 straight section



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500 mA Study, 2 BxB BPMs 5 Gapa data

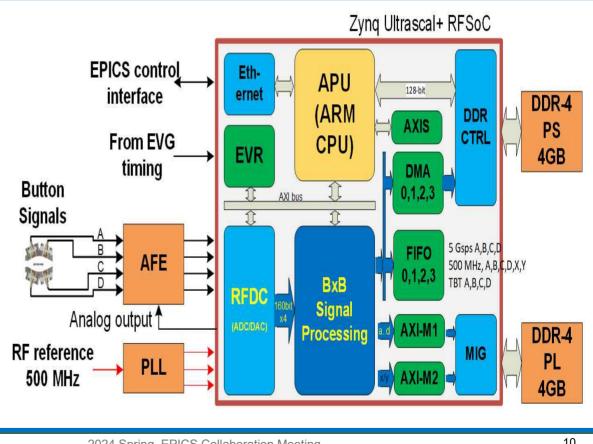


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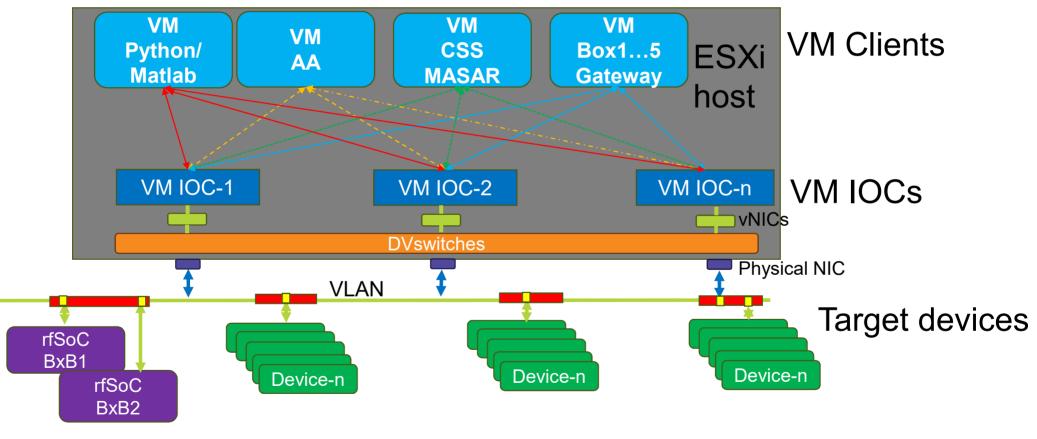
FPGA Firmware block diagram for applications

- AXI clock Fs/10 = 499.68 MHz (System locked with RF reference clock)
- ADC 5 Gsps A,B,C,D waveform stored BRAM 32 K points
- BxB 500 MHz A,B,C,D DDR-4 13.2 M*4 points (10 K turns, 105 Mbyte)
- BxB 500 MHz X/Y DDR-4 13.2 M • points (10 K turns, 26 Mbyte)
- Other BRAM for BxB waveform output and position.
- TBT 378 kHz A,B,C,D,X,Y BRAM 8 K points

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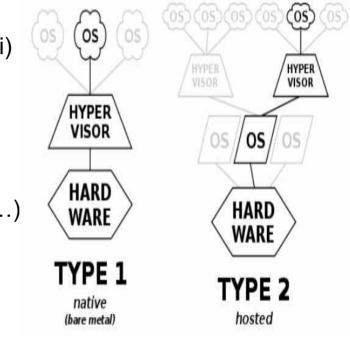
NSLS-II VM based accelerator control



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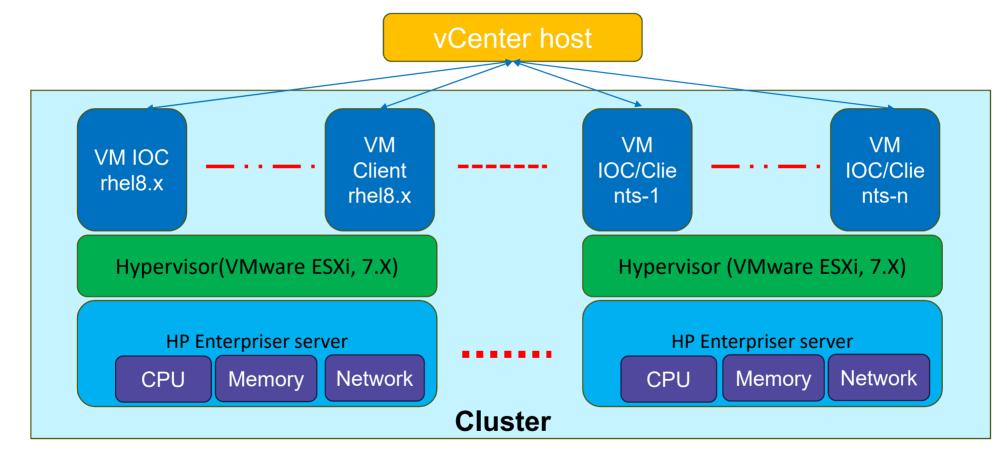
Hypervisor VM

- □ 2022-23 NSLS-II Control system upgrade to VM environments
- □ A hypervisor is computer software, firmware, or hardware that creates and runs virtual machines. Virtual Machine Manager(Wiki)
- □ Type-1 developed by IBM, In the late 1960s, and through the 1970s(CP/CMS: Control Program/Cambridge Monitor System)
 - □ Bare-metal hypervisors run directly on the hardware
- □ Type-2: hosted hypervisors (Vmware SW, Oracle VM VirtualBox...)
- □ NSLS-II used VMWare ESXi (enterprise class type-1 hypervisor)
- □ High-performance host computers and VMkernel
- □ Includes High-performance vSwitches, VMFS
- High availability (auto recovery)
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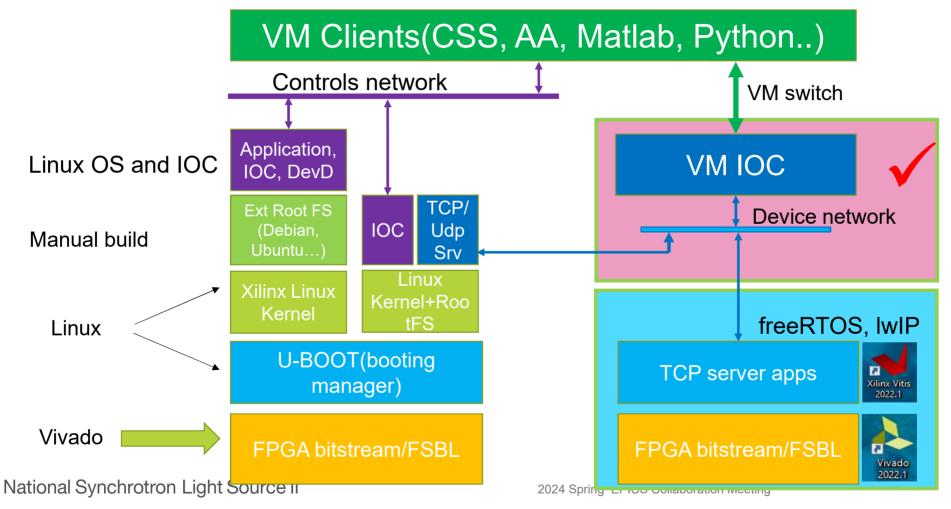
Source: wiki

Hypervisor and VM configuration(Type 1 - bear-metal) for IOCs and Clients



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VM-based control system interface



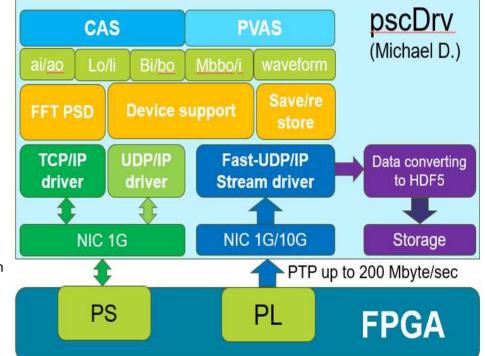
pscDrv IOC for FPGA interface

- Use NSLS-II in-house developed driver: pscDrv 2011~2022 (Michael D.)
 - **PSC = P**ortable Streaming Controller
 - Widely used at NSLS-II (PS, BPM, Active Interlock and Cell controller, APSu MPS, ALSu PS)
 - 2021 Update for APS-u project (improved UDP, high-speed UDP, saverestore...)

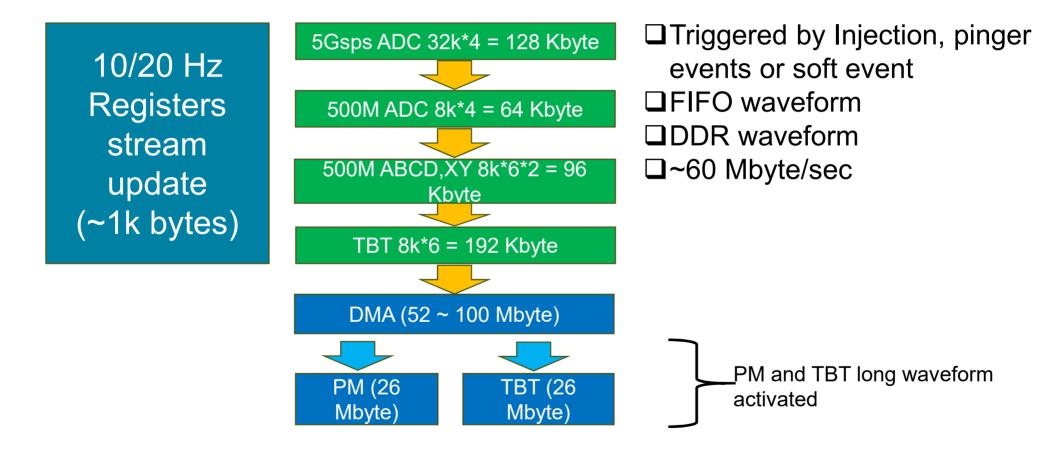
About pscDrv

- Single IOC supports many BPMs and target devices
- TCP/UDP/IP-based protocol
- Fast UDP for stream data saving (DAQ)
- Directly mapping with FPGA registers and memory (with CPU gateway)
- Not request messages and responses for communication (simple communication method)
- Scalar and array support
- I/O interrupt scan
- 32bit integer, 32/64bit IEEE floating point support
- Support EPICS 7.xx

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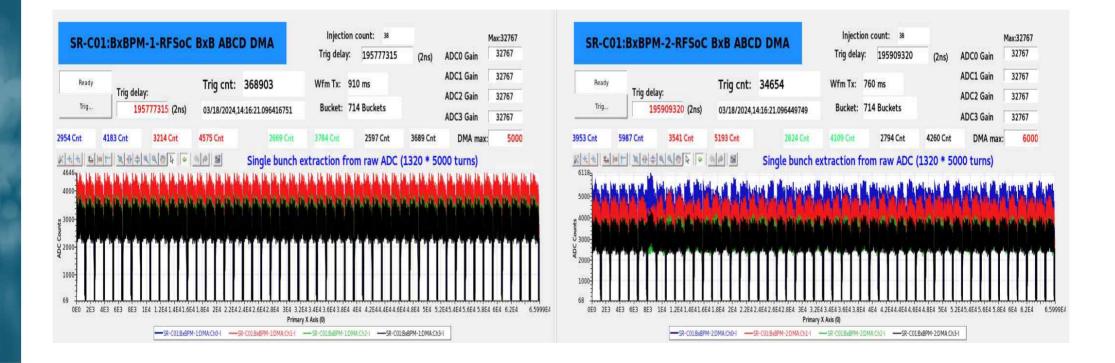


Scalar and Waveform update for data analysis



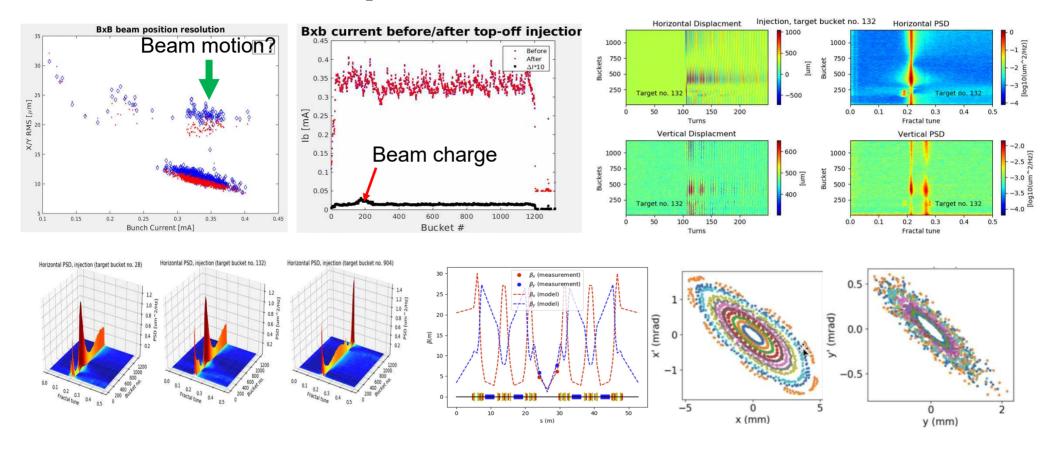
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BxB 500 MHz (1320*4*10k*2) 105 Mbyte



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Beam test examples



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Summary

- Deployed for beam operation and well-progressed beam study
- During top-off injection, available individual bunches measurement
 - Users satisfied performance
- VM IOC/Client and FPGA interface working well and stable (~60 Mbyte/sec)
- VM environment is a significant benefit for IOC and Client data transfer rate (< 1Gbyte/sec)
- The physics group working on extended user applications
- Moving forward to other applications (BPM, LLRF...)

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Thank you for your attention!

Questions and comments are welcome.

