PIP-II Beam Pattern Generator Upgrade

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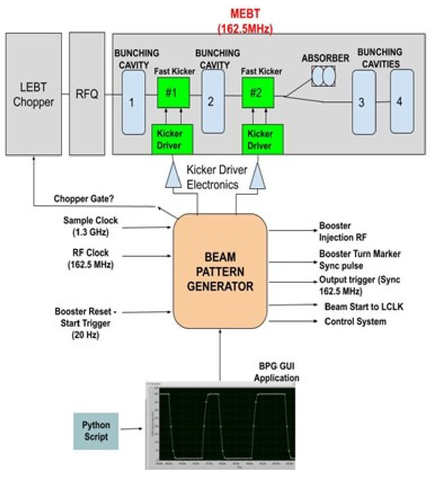
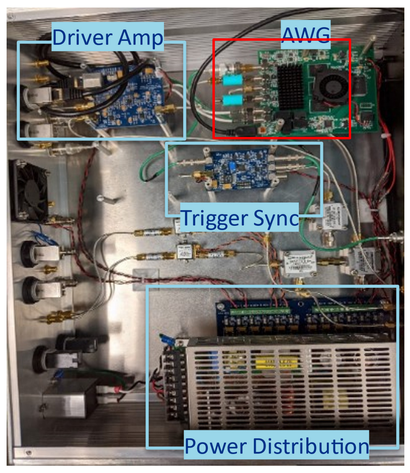
ID 26

Introduction

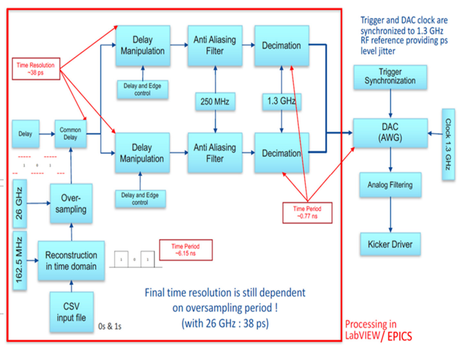
A prototype beam pattern generator for the PIP-II Linac testing used Labview and an external server for the pattern generation. A new design using a COTS sourced SoCFPGA and a DAC board offers the advantages of low hardware and development cost. The pattern generation, digital signal processing and the interface to an external EPICS server are integrated into the ARM processor of the FPGA. The system design is described and the test results are presented.

BPG Prototype



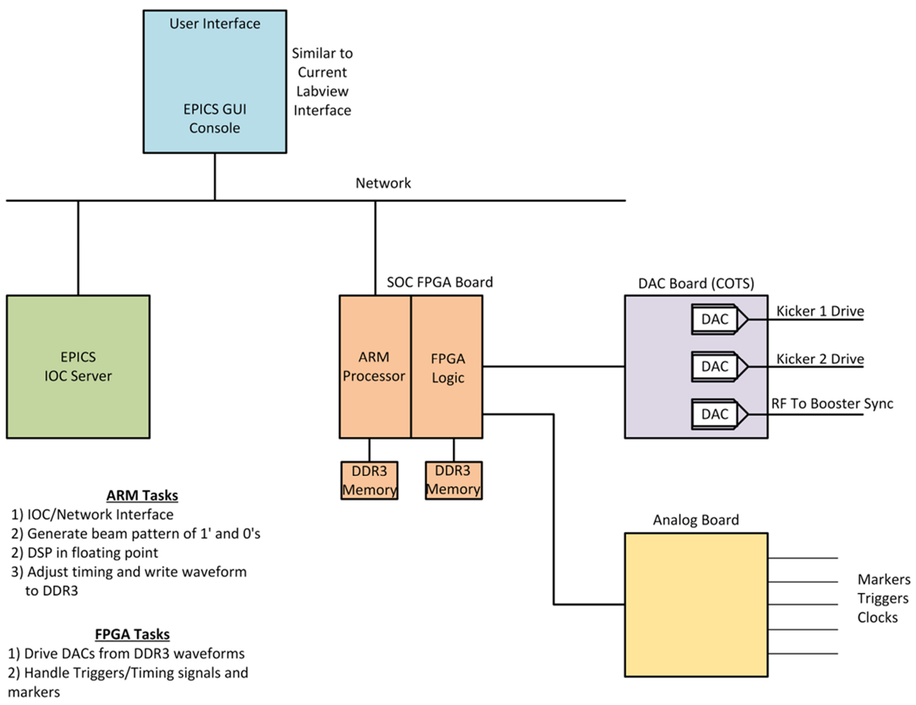


Signal Processing and Delay Adjustment



- Delay with respect to synchronized trigger
  - Compensate for cable lengths
  - Compensate for kicker driver delay
  - Internal delay of Arbitrary Waveform Generator (AWG)
- Differential delay
  - Different characteristics of kicker switches

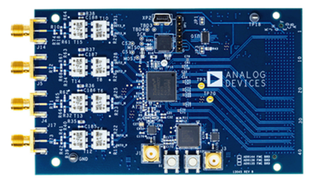
BPG Upgrade Architectuure



ARM Tasks
1) IOC/Network Interface
2) Generate beam pattern of 1' and 0's
2) DSP in floating point
3) Adjust timing and write waveform to DDR3

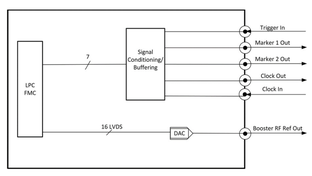
FPGA Tasks
1) Drive DACs from DDR3 waveforms
2) Handle Triggers/Timing signals and markers

Hardware Components



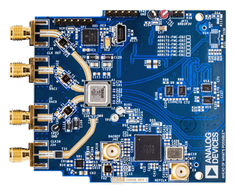
4 ch HS DAC Board
AD9144-FMCEBZ
16-bit, 2.8 GSPS, Ext Clk Input

Arria10 SOM



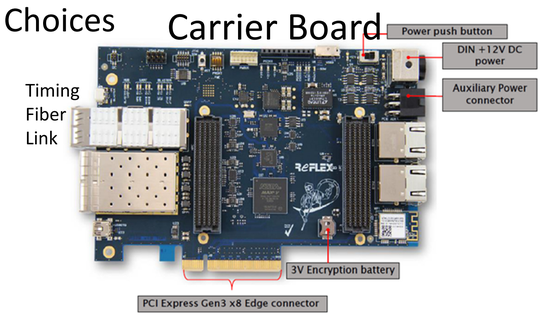
FMC Analog PCB

DAC Board –Multiple Choices

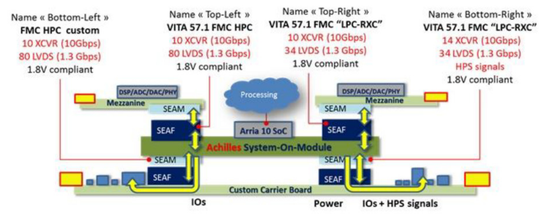


2 ch HS DAC Board
AD9172-FMCEBZ
16-bit, 12.6 GSPS, Ext Clk Input

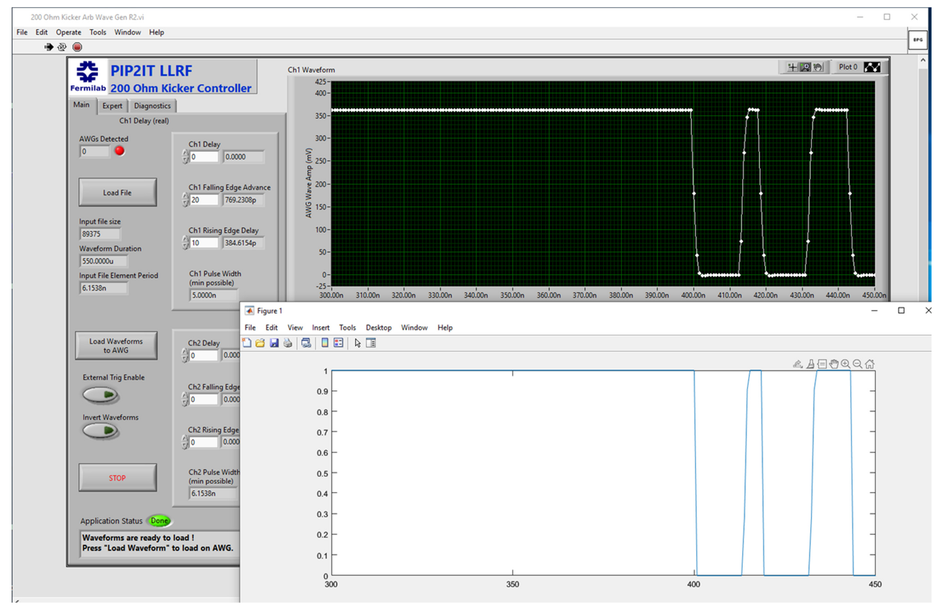
Carrier Board



Hardware Configuration



Pattern Generation and DSP – Labview vs ARM SOC



DAC Output Prototype

DAC Output SOCFPGA

Summary

- Major technical aspects for the upgrade already studied and demonstrated to work
- Tested Performance with prototype is guaranteed since the signal processing implemented is the same used at PIP2IT
- This upgrade is a joint project with SLAC

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