DIAMOND DIGITAL LOW LEVEL RF

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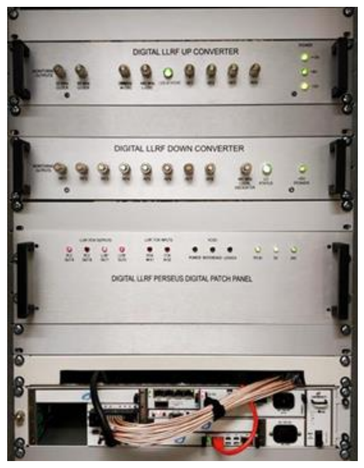
Introduction

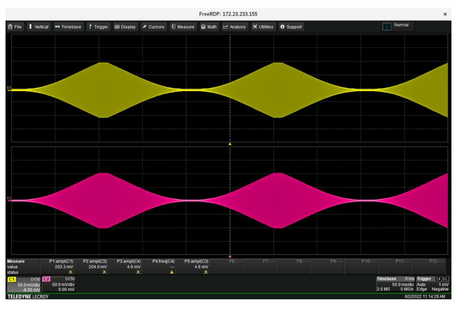
- The first version of digital low level RF (DLLRF) for the Diamond Light Source storage ring and booster was developed with ALBA Synchrotron. Six systems have been built so far. Two of them are in routine operation controlling two normal conducting HOM-damped cavities in the Diamond storage ring. A third system is being used for cavity testing in the RF test facility. The fourth system has been deployed to control the second normal conducting booster cavity. The fifth DLLRF system has been deployed this year for the third normal conducting RF cavity powered by solid state power amplifier in the storage ring.
- A new DLLRF system based on SIS8300-KU with RTM has been developed and tested in the last few years. The linac version with arbitrary waveform generator mode was tested successfully to generate flat top pulse from SLED at high power in the linac. The high-power pulse accelerated electron beam to 68 MeV in just one accelerating structure. DLLRF for passive harmonic cavity is being designed.

First Version DLLRF

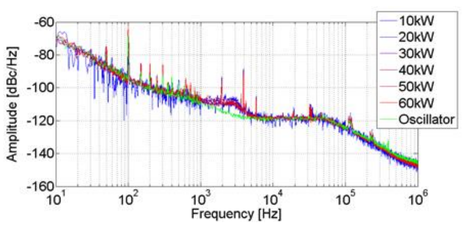
The DLLRF was based on the MicroTCA standard. Perseus 601X with Virtex6 FPGA from Nutaq, is used as the core processor of the control algorithm. 16 Channel 14-bit ADCs and 8 channel 16-bit DACs FPGA mezzanine cards (FMC) are used for analogue input and out interface.



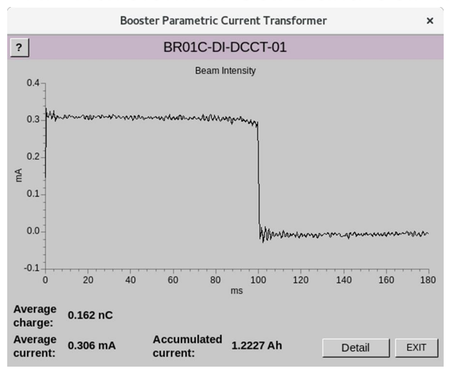
Installed DLLRF System.



RF Waveform in Cell 2 and Cell 4.



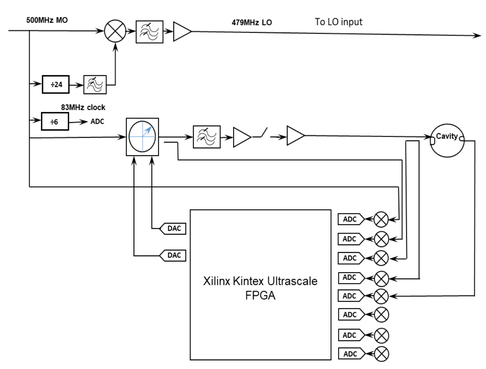
Measured Phase Noise



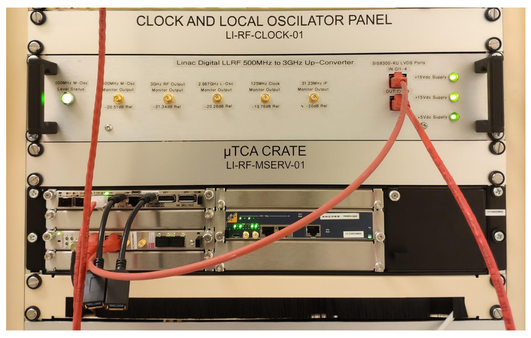
Accumulated Beam in Booster.
DLLRF for Second Booster Cavity.

New DLLRF

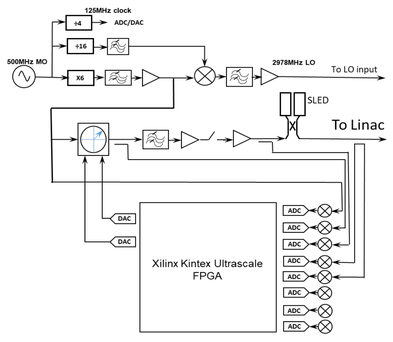
The new DLLRF consists of a 2U MTCA.4 chassis, a MCH, an AMC computer board, a Struck SIS8300-KU card, a Struck DWC8VM1 RTM with supporting clock/local oscillator (LO)/reference generation RF circuits. SIS8864 digital I/O card is being integrated into the system.



500MHz DLLRF System Architecture



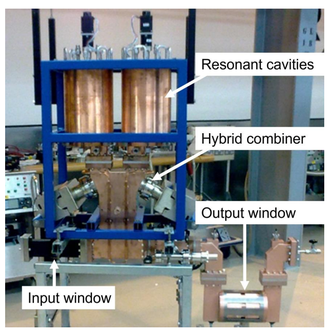
New DLLRF installed in Linac.



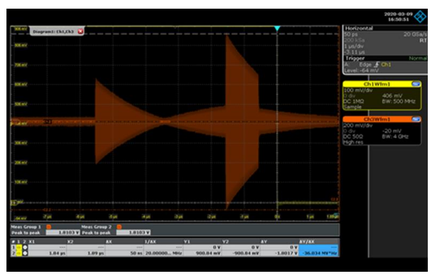
3GHz DLLRF System Architecture

DLLRF for SLED

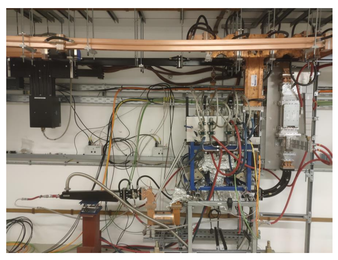
Three working modes were implemented in the firmware, namely standard mode, waveform and full arbitrary waveform mode. An external trigger is provided by the timing system through one of the two DC ADC channels. A long bunch train of 120 with 2 ns period was accelerated to 68 MeV using the flat-top pulse generated from the SLED.



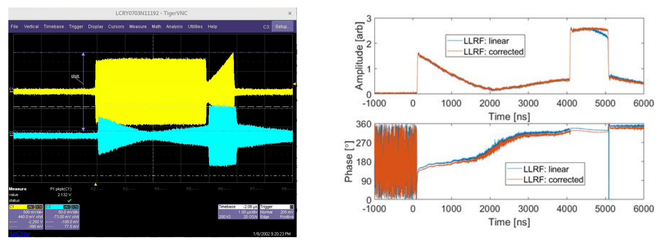
SLED



Standard Output Pulse from SLED



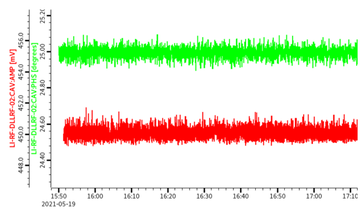
SLED Installed in Linac.



Flat-top Output Pulse from SLED

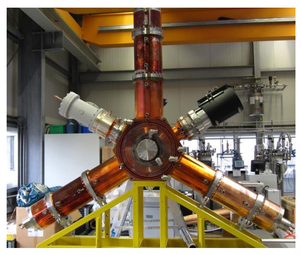
New DLLRF Tests on NC Cavity

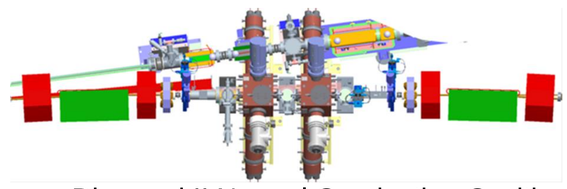
- This test includes the full chain of a RF system, that's DLLRF, solid state power amplifier and normal conducting RF cavity.
- All functionalities were tested.
- Achieved better than 0.1% in amplitude and 0.03 degree in phase with all the control loops closed while controlling normal conducting RF cavity.



Future Work

- New DLLRF for booster cavity 1 will be built, tested and deployed.
- DLLRF for high harmonic RF cavity will be designed.
- DLLRF for Diamond II normal conducting cavities will be built.





Diamond II Normal Conducting Cavities

References

[1] Pengda Gu, C. Christou et al., "Digital Low Level RF Systems for Diamond Light Source", in Proc. 8th Int. Particle Accelerator Conf. (IPAC '17), Copenhagen, Denmark, May 2017, pp. 4089-4091.

[2] C. Christou, P. Gu and A. Tropp, "Programmable SLED sys-tem for single bunch and multibunch linac operation", in 31st Linear Accelerator Conference, Liverpool, UK, August 2022