

Model Based Verification

for Multi-Cavity LLRF Control Systems

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Model Based Verification

for Multi-Cavity LLRF Control Systems

- > System Description
- > Development Workflow
- > Problem Definition
- > Model Based Solution
- > Status and Future Work

Multi-Cavity LLRF Control Systems

Plant and Hardware



Multi-Cavity LLRF Control Systems

Firmware

- Large number of sensor channels
- > Distributed architecture
- > Control action at 9 MHz with ~ 1 μs latency
- > Design optimization for quantization error to achieve tight regulation parameters
- > 20+ years support for various hardware
 - TCK7 (Kintex 7)
 - SIS8300L2 (Virtex 6)
 - RTM-uVM (Spartan 6)
 - PZ16M (Spartan 6)
 - TMCB (Spartan 6)
 - FMC25 (Virtex 5)



Multi-Cavity LLRF Control Systems

Software

LLRF Ctrl

- > Slow feedback control implementation
- > Manipulate fast feedback control (firmware)
- > Generate control tables (setpoint, feedforward, gain) for firmware
- Monitor sensor data and states of the controller
- > Manipulate parameters of hardware/firmware
- > Interface with **DOOCS.**



doocs.desy.de github.com/ChimeraTK



Requirements Specification

Long Term Goals Planning > 1 year



Algorithm Developer Perspective



Software Developer Perspective



Firmware Developer Perspective



Problem Definition

on Realization of a Controller in State Space



An Effective but Tedious Solution Bit and Cycle Accurate Modeling



Model Based Design

As a Complete Workflow



Co-Simulation

An Alternative to Manual Modeling of Design Behavior

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CO-SIMULATION OF HDL USING PYTHON AND MATLAB OVER Tcl TCP/IP SOCKET IN XILINX VIVADO AND MODELSIM TOOLS



(System)Verilog

External Language Interfaces for HDL

VPI (Verilog 2005, PLI 2.0)
VHPI (2008, 2019)

VHDL

DESY.MSK.FWK

An Open Source Firmware Development Framework



Open Loop Verification of the core FPGA IP for LLRF control





Future Work

Co-Simulation for Co-Processing



Thank you.

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