PAUL SCHERRER INSTITUT

Low Level RF Workshop 2023

Signal processing architecture of the next generation LLRF systems at PSI

R. Rybaniec[1], <radoslaw.rybaniec@psi.ch>, B. Stef[1], R. Kalt[1], A. Dietrich[1]

[1] Paul Scherrer Institut (PSI), Dept. Large Research Facilities (GFA), CH-5232 Villigen PSI, Switzerland

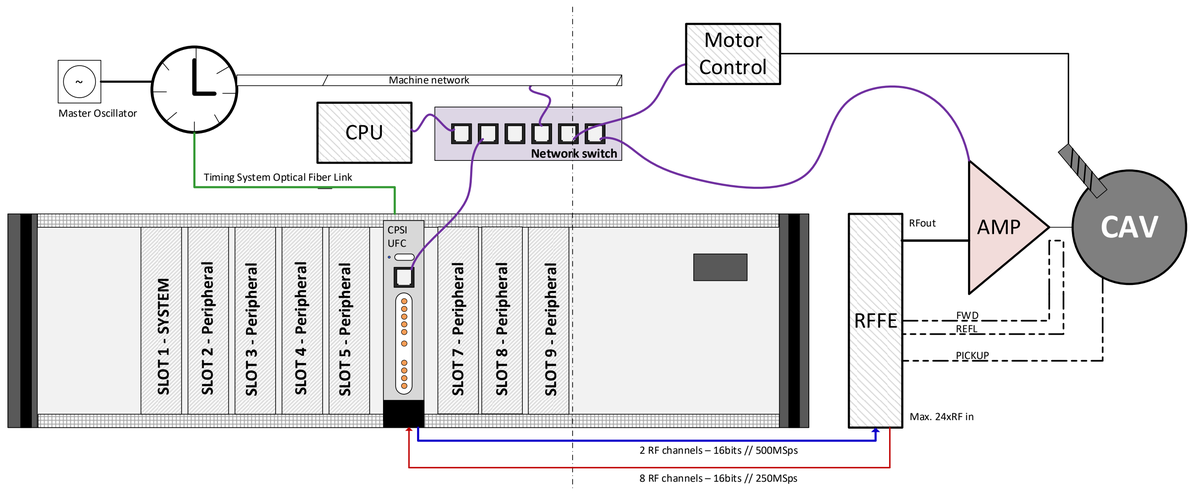
Abstract

LLRF systems play a crucial role in the efficient operation and control of particle accelerators. At the Paul Scherrer Institute (PSI), advanced LLRF systems are being developed to meet the demands of upcoming facility upgrades, including Swiss Light Source (SLS) and High Intensity Proton Accelerator (HIPA). In this contribution, we present the signal processing architecture designed for these next-generation LLRF systems.

Always and independent of the machine or operation type, digital LLRF systems share the same key functions: Data acquisition (DAQ), RF actuation and feedback control. In addition, some management and automation features including exception handling and state control are required. Finally, LLRF systems typically interoperate with others systems, such as timing and machine protection.

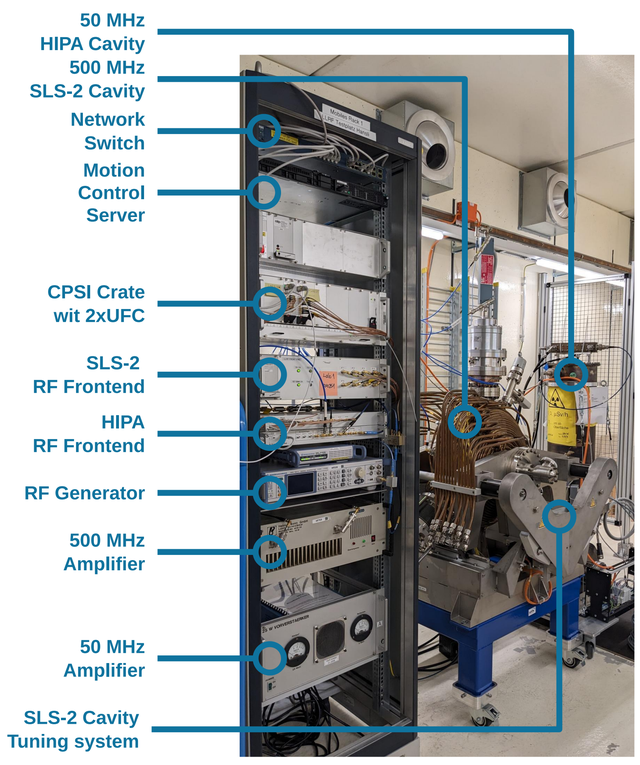
As an example architecture implementation, we present the design of the SLS-2 500 MHz LLRF, which is intended for CW and pulsed RF operation. The LLRF features are divided into different architecture layers, including programmable logic, embedded software, and the high level control system. Where applicable, re-usable and universal library elements are used.

Hardware architecture



Both SLS (500 MHz) and HIPA (50 MHz) LLRF systems share the same hardware architecture. CompactPCI Serial[1] is the base for FPGA processing system. One pair of Universal FMC Carrier/DAC Rear Transition Module boards (UFC/DAC-RTM) provides MPSoC for real-time signal processing and communication purposes, as well as 8 ch. 16bit 250Msps ADC and 2 ch. 500Msps 16 bit DAC for RF signals I/O. External LLRF frontend (RFFE box) provides IF signals for digitizer and its design is customized for the specific facility. Cavity resonance tuning, statistics computation and other non real-time algorithms run on an external CPU connected via Ethernet.

Teststand

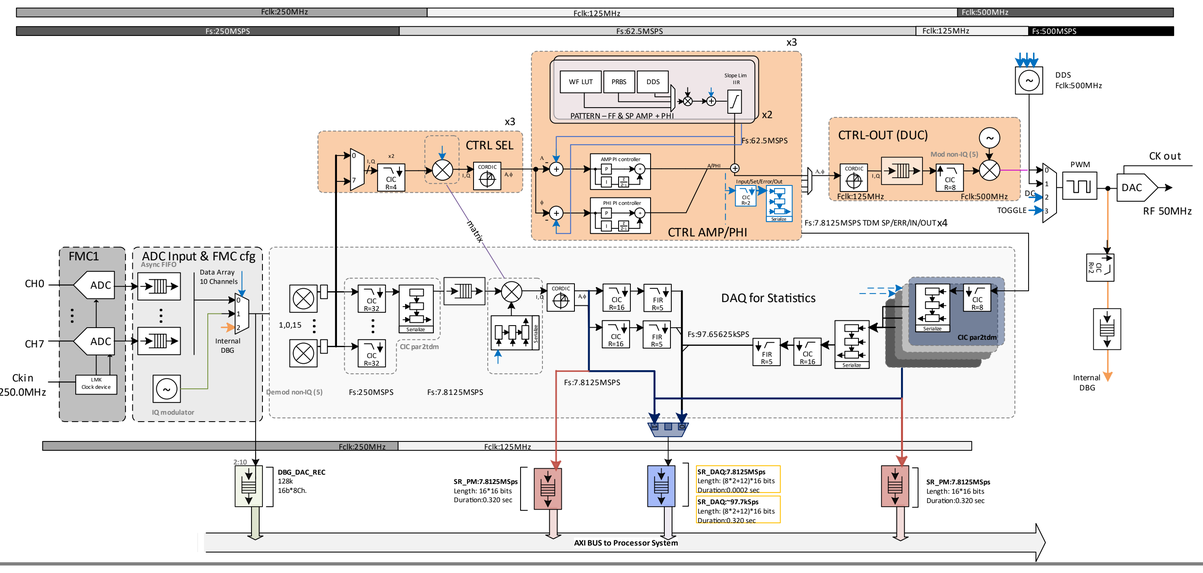


In 2023 a new LLRF test stand has been commissioned (left). It is equipped with two independent systems running in parallel (HIPA's 50 MHz buncher cavity and SLS's 500MHz cavity). Both systems are equipped with motor controllers for tuning and RF amplifiers for performing low power tests. They allow for comprehensive tests closer to the operational conditions than initial tests performed in 2022 (below).

FW/SW architecture

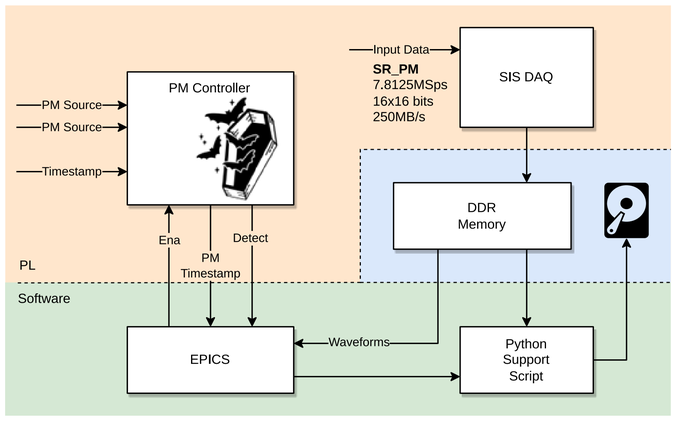
The design of LLRF SLS-2 FW is mainly composed of reusable blocks from PSI libraries (qr-code).

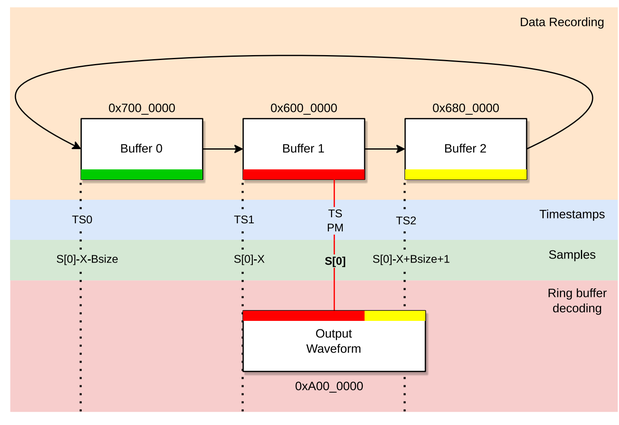
3 PI controllers based on pick-up, forward and reflected signals are running in parallel. A coordinator module (not included in the current FW) will select one active controller according to the cavity state. Besides feedback controllers, the FW provides a set of feed forward modulation schemes (arbitrary shape, sine wave, PRBS, etc.) that are used for cavity conditioning and system identification. Utilisation of MPSoC allows running an EPICS server and LLRF applications on the same chip. FW and SW reuse the identical Board Support Package as other PSI applications.



Post Mortem Data Acquisition

Post Mortem Data Acquisition (PM DAQ) is implemented using both programmable logic (PL) and software part. The controller component in PL generates a detect signal when one of the input sources gets active. The source which caused a PM event together with a timestamp is provided. Data are continuously recorded into DDR memory by using triple buffering scheme. The detect signals stops the acquisition in such a way that the sample 0 is recorded in the central buffer. Timestamps are extrapolated for each samples in the buffers which allows for assembly of the output buffer with desired pre-trigger and post-trigger sample numbers. A short subset of the samples is displayed on the panel for the user with an option to store all available data in the archiver.





References: [1] B. Stef et al., "CompactPCI Serial Based Generic and Modular Processing Platform at PSI", LLRF Workshop 2022, Brugg, Switzerland.

Acknowledgments: Thanks to all PSI AEK members that took part in the development especially to R. Biffiger, D.Felici, I. Johnson, W. Koprek & L. Moser for their great contributions and M. Pedrozzi for review and comments.

Conclusion

The new processing platform developed at PSI is versatile and supports needs of different facilities with minimum modifications. It allows rapidly to develop new functions covering demanding user requirements by reusing generic hardware, firmware and software elements. Available MPSoC allows for concentration of the LLRF functionality on one digital board which improves maintainability, ease the integration by reducing interface complexity, and improves observability by providing more data sources for analysis, in comparison with its predecessors.