New RFPI system for the PIP-II accelerating structures

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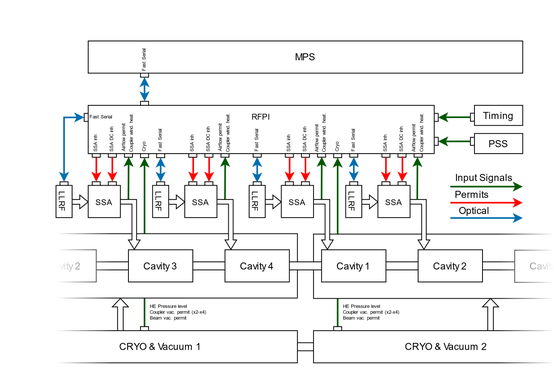
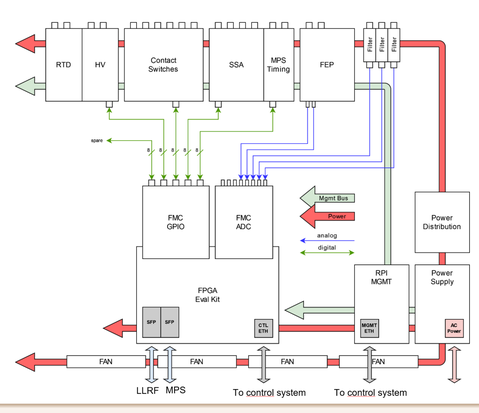
Abstract

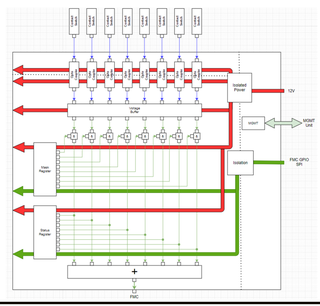
The cryomodule or cavity data like vacuum status, helium level, RF leakage level, field emission probe signal and others can be important indicators of of conditions that could compromise the stable operation of the RF systems including amplifiers, RF distribution, fundamental power couplers, and superconducting accelerating structures.. That is why the dedicated system (RF Protection Interlock - RPFI) has to closely monitor all sensitive parameters and drop the permission for RF operation instantaneously when a possible fault situation occurs. The new design of such an RFPI system has been proposed by LUT-DMCS team. This system is dedicated to the PIP-II accelerating structures. The modular design and interlock logic realization by the SoC (system on Chip) module are the main driving factors for this development. Such an approach provides not only a fast reaction to upcoming faults but also wide flexibility in the input signal sets and protection logic configuration and implementation. This contribution describes the proof of concept prototype design and evaluation as well as the full signal count prototype ongoing efforts.

RFPI prototype structure





Signals conditioning modules

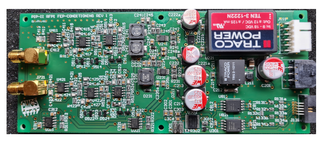


Contact switches signal conditioning module

- monitoring of open/close PLC switches inputs,
- different voltages depending on the switch type (12/24V),
- equipped with cable open/short diagnostics,
- equipped with a single signal latching,
- configurable NC or NO behavior,
- 8 channels available on the PoC version.

The FEP signal conditioning module

- ready for 2 e-pickup channels,
- adjustable biasing voltage level up to 45V via SPI,
- current detection in the range of micro ampere



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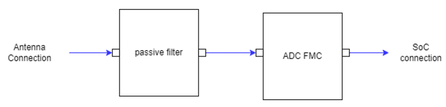
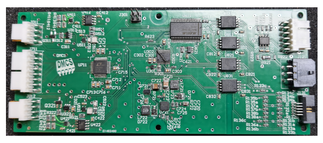


The Non-ionising Radiation Probe - NIRP .

- different bans-pass filters verified 162.5, 325 and 650 MHz,
- for PoC: up to 4 RF detectors can be configured - 4 channels monitoring

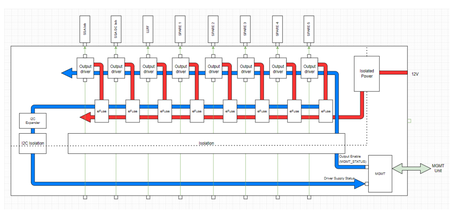


The Resistance Temperature Detector (RTD) and Coupler Bias High Voltage Power Supply SC

- two temperature measurement channels available,
- ready for four wires configuration operation,
- High Voltage power supply voltage and current read-out,

The SSA outputs/inputs signal conditioning module

- SSA, SSA DC, LLRF, MPS permit output signal generation,
- SSA ready input signal,
- equipped with e-fuse (thermal fuse) protection.



Management and Diagnostics sub-system

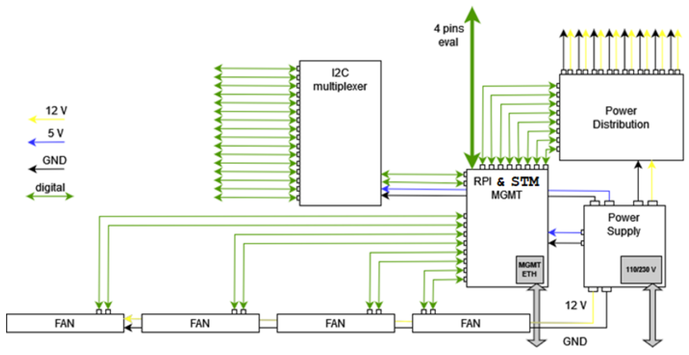


Figure 1: PoC Management subsystem

- provides watchdog mechanisms for main logic unit,
- generates "system health" signal,
- provides the FPGA chip firmware upload and debugging.
- collects data from the voltage, current, and temperature sensors,
- execute protection procedures for RFPI (overheating, over-voltage),
- controls supply voltage for each part of the RFPI,

Acknowledgements

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HW structure - Main logic unit and FMC modules

Main logic unit

- ZCU106 (by Xilinx) eval board - carrier,
- Zynq UltraScale+™ FPGA chip and a quad-core Arm Cortex A53
- two FMC slots
- FPGA - main logic function implementation,
- Arm processor - EPICS integration and IOC for configuration and inputs / outputs monitoring

FMC modules

- FMC GPIO with 40 GPIO channels for SC interfacing,
- acceptable throughput - up to 50MHz,
- FMC ADC for analog (and RF) signals,
- 8 channels (14-bits, 25 MS/s),
- equipped (optionally) with RF detector

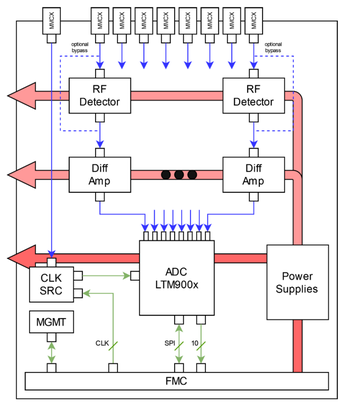


Figure 2: FMC ADC module structure diagram

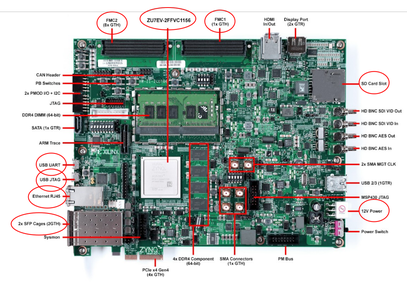


Figure 3: Main logic unit - evaluation module (https://www.xilinx.com/products/boards-and-kits/zcu106.htmlinformation

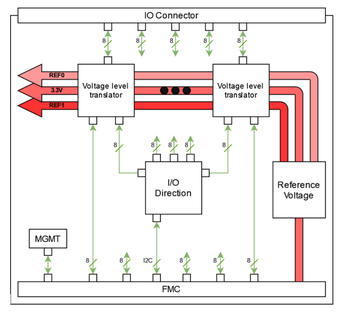
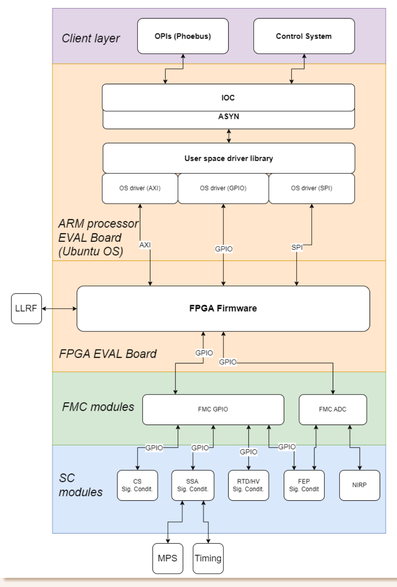
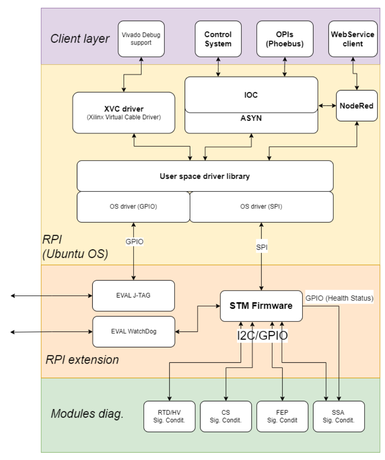
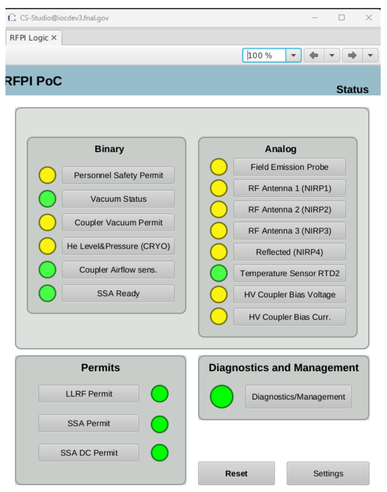


Figure 4: FMC GPIO post-production view

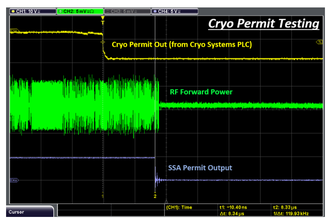
Software structure

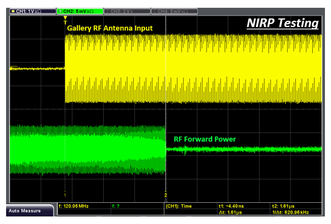






Prototype verification





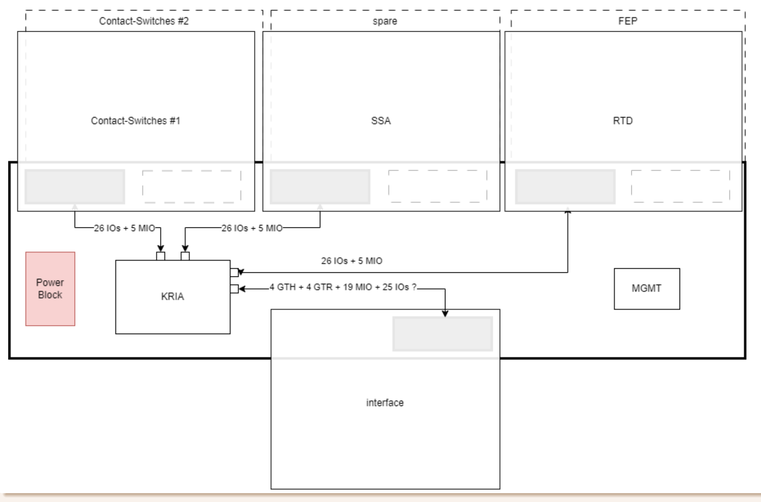
The test-bench verification

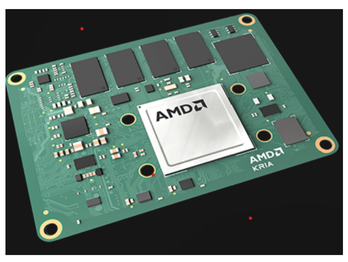
- SC modules post-production testing - individual channel confirmation,
- PoC box after integration testing - main protection function logic checks,
- system modules design improvements introduced based on findings from bench verification.

PIP2IT verification

- the PoC integration and operation with cavities in the high beta (HB650) cryomodule,
- the RFPI PoC response performance measurement (from artificial fault occurrence to RFPI permits drop),
- achieved performance better than defined in requirements,
- several hours of successful "in the loop" PoC operation dedicated to single cavity protection

Full-scale prototype development





source: http:www.xilinx.com

- Carrier board with SoM (Kria26),
- 6 FMC slots for signal conditioning,
- FMC based interface board,
- dedicated management chip (integrated on carrier).