Dual Frequency Master Oscillator Generation and Distribution For ALS and ALS-U

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Abstract

The ongoing work to upgrade ALS to ALS-U demands strict RF requirements such as low jitter and low spurs frequency reference to meet its accelerator and science goals. A low phase noise dual frequency Master Oscillator (MO), where the two frequencies are related by a fractional ratio of 608/609 and flexible divide by four frequency outputs has been consolidated into a single chassis. Optical fiber clock distribution system has been selected over the old coax system used in ALS to distribute these signals to various clients across the facility, providing high electrical isolation between outputs and therefore lower phase errors. A Xilinx FPGA ties the MO chassis together by providing a RS-485 interface to monitor and control the system. The new system aims to deliver phase continuous frequencies with a phase noise (integrated RMS jitter) from 1 Hz to 1 MHz of less than 200 femtosecond per output. This paper will discuss the design, implementation, performance and installation of the new MO generation and distribution system.

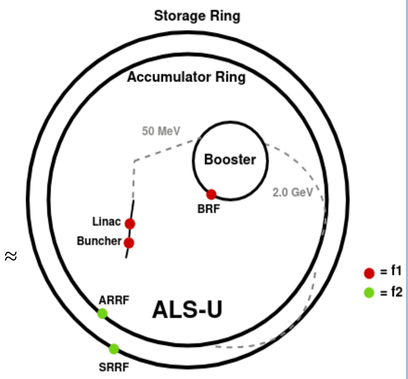
Introduction

Legacy MO system at ALS

- Encapsulation of crystal oscillators, distribution amplifiers to provide f2 ≈ 400.64 MHz using phase-stable coaxial cables.
- AD9513 evaluation board - generate divide by four frequency.
- Original parts from 1989 are now obsolete.
- Beamline experimental setups - require lower phase noise and are more sensitive to spurs.
- Existing distribution chassis - adds phase noise to the reference signal.

Upgrade from ALS to ALS-U

- Installation of new Storage Ring (SR) and Accumulator Ring (AR) at ALS-U will increase the MO RF frequency to f2 ≈ 500.39 MHz, and a choice was made to operate them along with the beamline at this frequency.
- Linac and Booster operates at a new lower frequency, f1 = f2*(608/609) ≈ 499.56 MHz.
- Current coax based MO distribution system is not flexible to support this new dual frequency configuration.



Installation & Commissioning

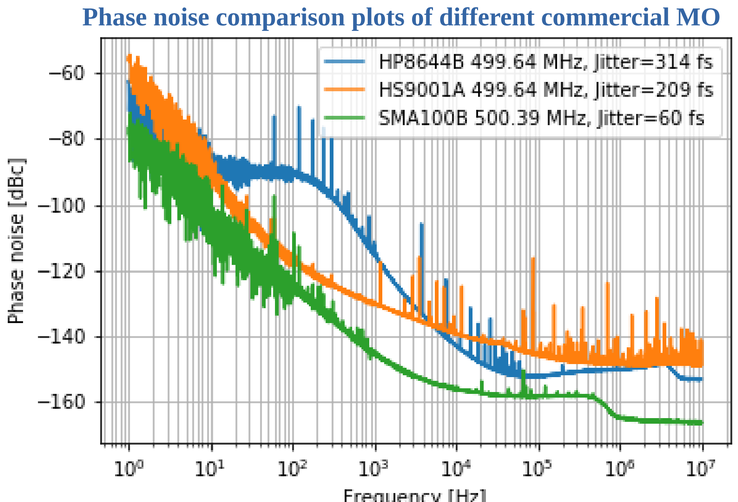
Installation in three stages over next few years

- Pre-Dark Time - divided into two stages, before AR and during the AR commissioning periods.
- Post-Dark Time - final ALS-U configuration in 2025.

Changed hierarchical crystal oscillator source to commercial signal source - achieve lowest phase noise and spurs.

- Crystal oscillator → HP8644B → HS9001A → SMA100B

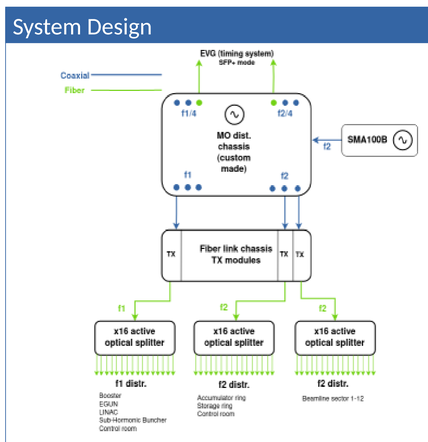
Phase noise comparison plots of different commercial MO

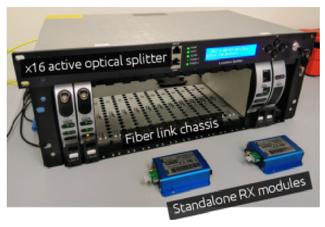


September 2023 summer shutdown

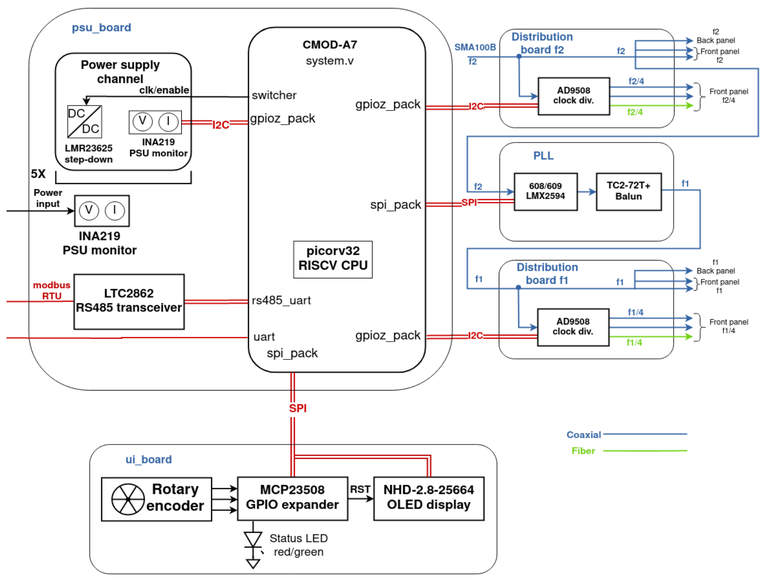
- Installed - Distribution chassis, Vialite fiber link chassis, and three Vialite splitters.
- Two clients: f1 coax output - to the entire system through the old MO distribution system and the 1/4 divider, f1 fiber output - to the Sub-Harmonic Buncher (SHB) through the Vialite system.
- Next commissioning phase - old distribution system with the 1/4 divider will be retired. The new proposed system will drive the entire accelerator.

System Design





- Commercial ultra low-noise SMA100B (MO) - generate f2 @ 500.39 MHz.
- Custom build chassis - generate f1 = f2*(608/609), f2/4 and f1/4 and distribute them along with f2.
- Optical fiber system (RFoF) - fiber link chassis and active optical splitters.
- 2x Distribution boards with AD9508 - one for each f1 and f2.
- 1x LMX2594 PLL evaluation board - generate 608/609*f2 = f1.
- 1x Power Supply Unit (PSU) board - power management, control UART and Modbus communication, frequency counters.
- 1x CMOD-A7 FPGA module.
- 1x User Interface (UI) board - user interface and display.

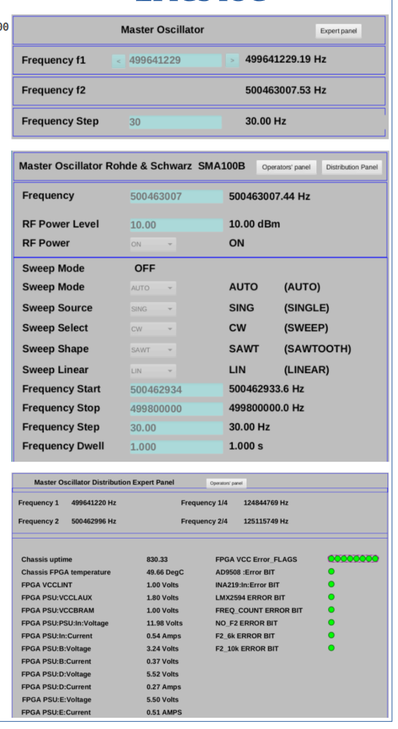


- Open-source, size-optimized RISC-V CPU PicoRV32 - handles system configuration, boot-time self-checking, continuous status monitoring, and remote interfacing with EPICS via the RS485/Modbus RTU port.
- Firmware supports serial communication protocols through the PMOD connectors - SPI to communicate to the PLL and the UI boards and I2C to communicate to the AD9508 clock divider chip.
- Four frequency counters with 500 Hz accuracy - f2, f1, f2/4 and f1/4.
- Host server continuously polls registers through the interrupt service function of the PicoRV32, retrieves real-time register information for monitoring.
- Available registers - voltage and current monitoring, continuous error detection (communication error, PLL not locked, and f2 frequency drifts), and frequency counters.
- UI board - displays these status registers through the OLED screen.
- EPICS IOC built based on this register mapping.
- Phoebus engineering screen - display both the MO and the distribution chassis status at both operator and expert level panels.
- Archived frequency data available for long-term study.

Chassis testing and initialization

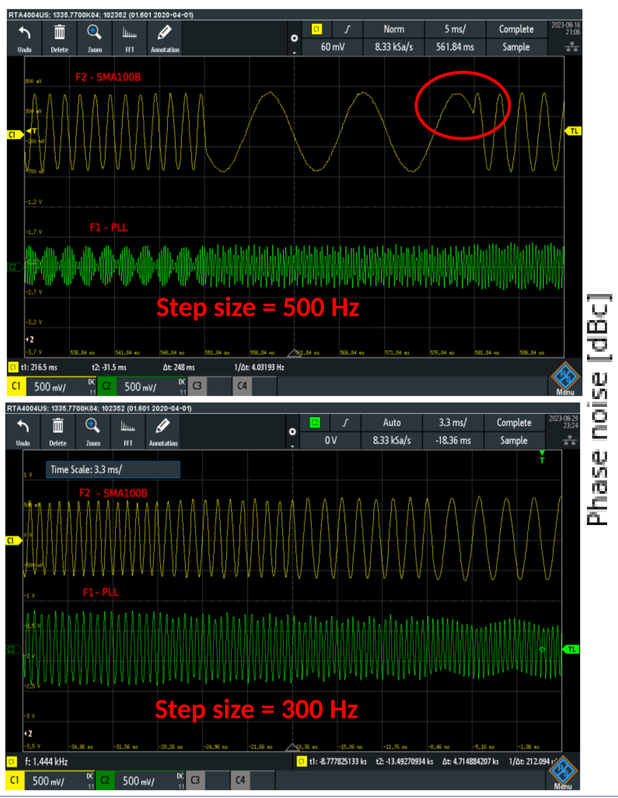
```
^[[Ashree@shree-ThinkPad-X1-Carbon-Gen-8:~$ miniterm /dev/ttyUSB1 115200
--- Miniterm on /dev/ttyUSB1  115200,8,N,1 ---
--- Quit: Ctrl+] | Menu: Ctrl+T | Help: Ctrl+T followed by Ctrl+H ---
ook

psu_board


AD9508 Address 6D
I2C scan: [6D ]
ID: 0005, REV: 02
 AD9508 init success!

AD9508 Address 6C
I2C scan: [6C ]
ID: 0005, REV: 02
 AD9508 init success!

LMX2594 init ...
 LMX2594 lock detect: 1
 LMX2594 init success!

 All the frequency counters are valid, within 20.0 ppm

I2C scan: [00 40 41 42 43 44 45 ]

    0000: 0000 2DD9 03E7 0707 03E9 2E74 01F4 1754
    0010: 0005 0C9C 0180 0C9C 0001 159C 010A 1580
    0020: 01AB 0000 0000 0000 0000 0000 0000 0000
    0030: 0000 0000 0000 0000 0000 0000 1DD4 76A0
    0040: 1DC7 EC8C 0775 1DA8 0771 FB23 001F 6DC5
    0050: 0000 3333 6666 0000 0000 0000 0000 0000
    0060: 0000 0000 0000 0000 0000 0000 0015 0000
    0070: 0000 0000 0000 0000 0000 0000 0000 0000

psu_board
?   This help
m   modbus register dump
i   chassisInit() to clear errors
+   Increase LMX2594 F1 amplitude level
-   Decrease LMX2594 F1 amplitude level

        PSU_UP:     0.0 h
 PSU_ERR_FLAGS: 0000
PSU_IN_VOLTAGE: 11892 mV
PSU_IN_CURRENT: 500 mA
        F1_PWR: 21 counts
       F2 Freq: 500.463260 MHz
       F1 Freq: 499.641484 MHz
      F2/4 Freq: 125.115815 MHz
      F1/4 Freq: 124.910371 MHz
```

EPICS IOC



Performance

Phase and amplitude continuity test while frequency sweep: SMA100B and LMX2594 PLL continuous with step size < 300 Hz



Measured phase noise and spurs of the new MO system at every output stage: Jitter < 200 fs [1 Hz - 1 MHz frequency range]. No significant spurs in 1 Hz to 100 kHz offset range.

Conclusion

- New dual frequency MO system with single generation and distribution chassis and fiber technology designed, and installed at ALS.
- Phase and amplitude is continuous for step size < 300 Hz.
- Measured phase noise from 1 Hz to 1 MHz is < 200 fs.
- A spare SMA100B and distribution chassis will be deployed in the lab for Continuous Integration (CI) and to produce reference for the sub-systems.
- Optimization of PLL loop filter can be easily achieved if requirements change during the final ALS-U commissioning.

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