LLRF system considerations for a compact, commercial C-band accelerator using the AMD Xilinx RF-SoC

Abstract

This work describes the LLRF and control system in use for a novel accelerator structure developed for a compact design operating in C-band developed by SLAC, with collaboration from RadiaBeam and RadiaSoft. This design is a pulsed RF/pulsed beam system that only provides minimal monitoring for control of each two-cavity pair. Available signals include only a forward and reflected signal for each pair; such a design requires careful consideration of calibration and power-on routines, as well an understanding of how to correct for disturbances caused by the entire RF signal chain, including a new SSA, klystron, and distribution system. An AMD Xilinx RF-SoC with a separate supervisory computer is the LLRF system core, with on-board pulse-to-pulse feedback corrections. This work presents the current status of the project, as well as obstacles and manufacturing plans from the viewpoint of developing for larger-volume manufacturing.

Background

The system is planned as a portable accelerator with the capability of operating on battery. In order to achieve this, we want to minimize the power used by each component, with the RF-SoC device using the majority of its power for the RF components. Proper power management should enable significant savings while the LLRF system is in standby or asleep.

In order to minimize cabling and system complexity, minimal RF signals are available for control and monitoring. The systems architecture consists of a single forward and reflected probe for each cavity pair, requiring back-calculation to get the magnitude and phase of the field. A robust, simplified simulation framework was developed to allow for online algorithm testing.

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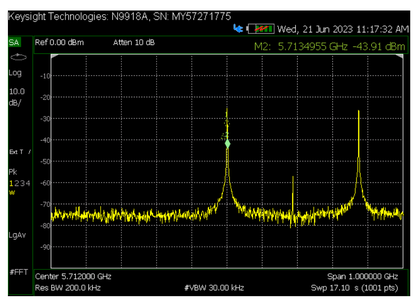
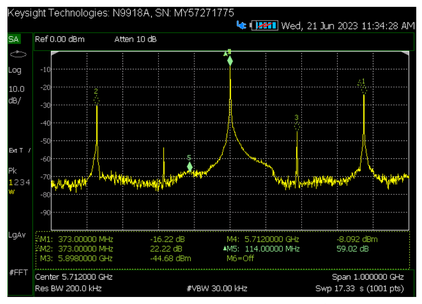
System Testing

The prototype LLRF system was tested with cavities in lab testing at SLAC and at high power in a RadiaBeam test bunker. Testing is complicated by the need to share a single klystron between two test caves. This involves the use of a high-power phase shifter developed at SLAC. The SSA is still undergoing refinements in its design to be more reliable, in particular for pulsed operation. A spectrum at the output of the SSA, when driven by the RF-SoC, shows images of the fundamental, as well as spikes at the sampling frequency.



Spectrum at output of RF-SoC



Spectrum of SSA with RF-SoC drive

Simulation

A full-featured, simplified-model RF simulator was developed to derive control algorithms and characterize system performance. Controlling two cavities with minimal control and monitoring requires a complete understanding of the signals being seen, as well as being able to understand signal performance in the presence of detuning or errors.

Listing all free parameters of a single element

```
Simulator Actions:

        1) Run a simulation
        2) List all LLRF elements
        3) List all free parameters of an element
        4) Change a free parameter of an element
        5) Load a new configuration file
        0) Exit

Please choose an option from the menu
-> 3
Name of the LLRF element:
-> Gen

Parameters of element 'Gen'
```

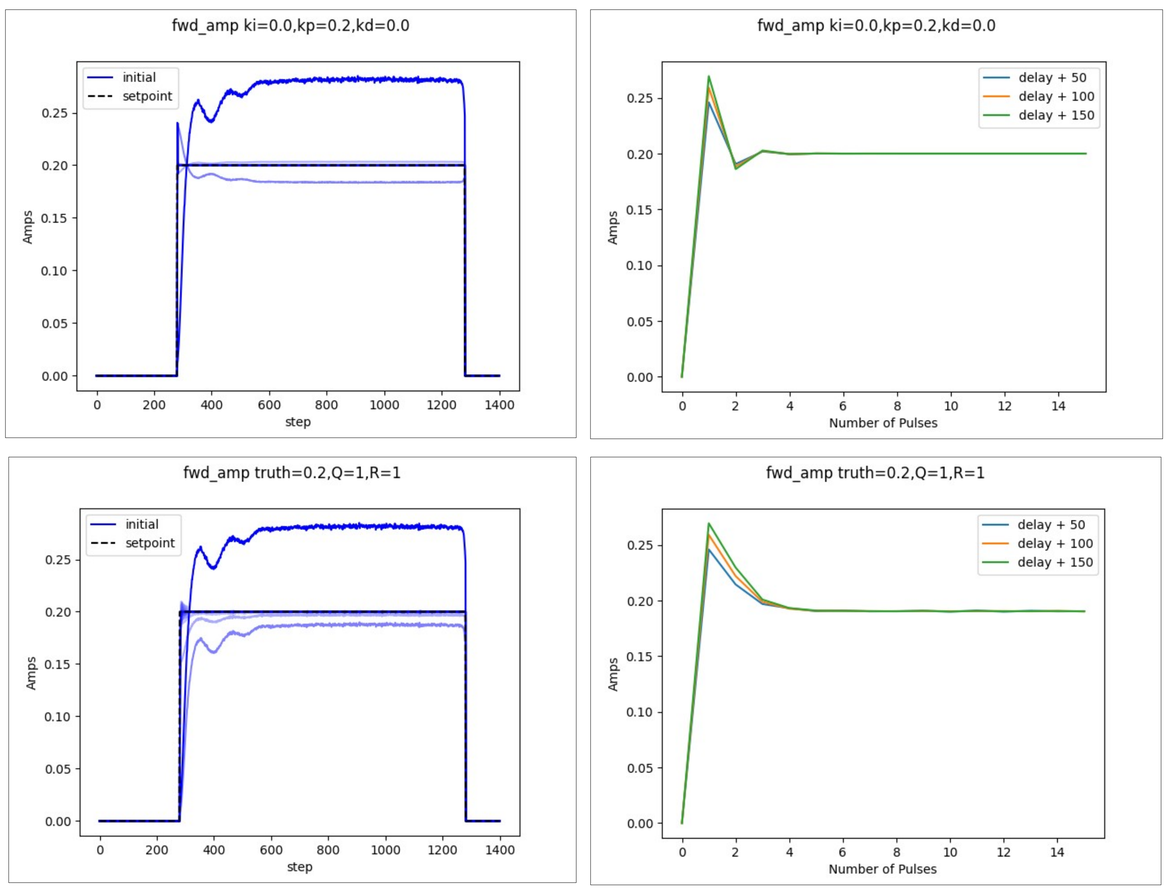
Parameter	Value
phase	0.0000
signal_type	tophat
signal_params	{'amp': 0.003, 'start': 2.5e-07, 'duration': 3e-06, 'rho': 250000000.0}

Listing all elements in the system

```
Simulator Actions:

        1) Run a simulation
        2) List all LLRF elements
        3) List all free parameters of an element
        4) Change a free parameter of an element
        5) Load a new configuration file
        0) Exit

Please choose an option from the menu
-> 2

LLRF Elements
```

Name	Type	Port Connections
Gen	Generator	1: GenTee
Beam	Beam	1: Cav1 2: Cav2
GenTee	Line	1: Gen 2: Tee
Tee	MagicTee	1: GenTee 2: TeeLoad 3: TeeCav1 4: TeeShift
TeeLoad	Line	1: Tee 2: Load
Load	Load	1: TeeLoad
TeeCav1	Line	1: Tee 2: Cav1
Cav1	Cavity	1: TeeCav1 2: Beam
TeeShift	Line	1: Tee 2: Shift
Shift	Shifter	1: TeeShift 2: ShiftCav2
ShiftCav2	Line	1: Shift 2: Cav2
Cav2	Cavity	1: ShiftCav2 2: Beam

A key feature of the system is also an ability to correct for inter- and intra-pulse variations to correct system non-linearities and perform within the design requirements. Several control algorithms have been tested using our closed-loop simulator, including PID and Kalman methods.

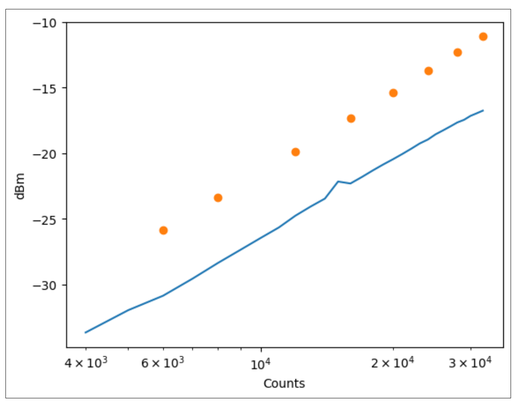


Top: results of PID pulse-by-pulse simulation; Bottom: Results of Kalman filter pulse-by-pulse simulation

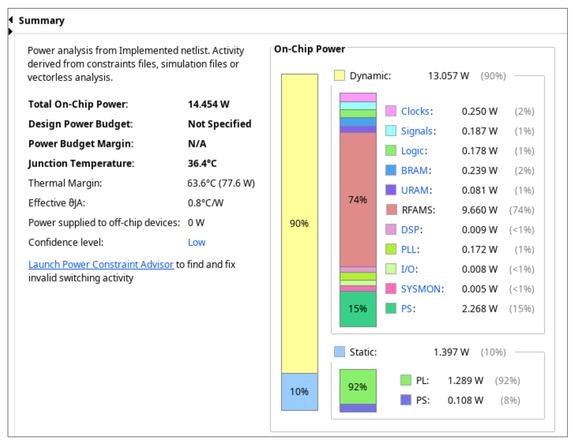
Power Considerations

Due to the choice of sampling frequencies and DAC settings, an image of the fundamental frequency of equivalent power output is in the adjoining Nyquist zone. This can be seen in the difference in RF output power measurements depending on technique (FFT or power meter).

The LLRF system power is dominated by the RF-SoC ADC/DAC subsystem, with more than two-thirds of the device power used by the device IP.



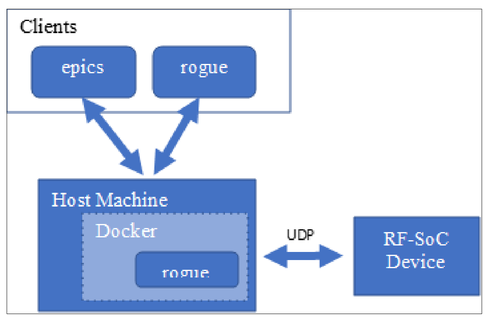
Power map of ZCU216 evaluation kit DAC output in counts vs measured power. Blue line is power measured using an FFT on a fast scope, orange dots are power as measured by a peak power meter.



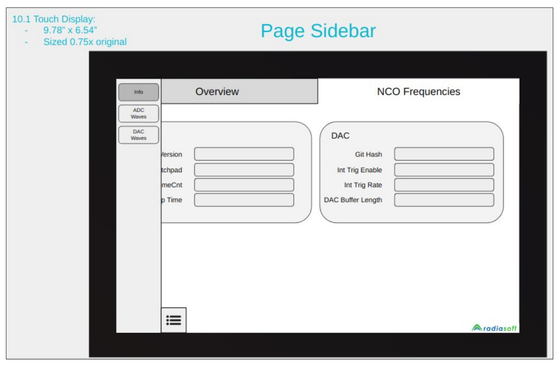
Vivado power estimation for implemented RF-SoC design

RadiaSoft is also responsible for developing a high-level controls interface for the entire system. This is planned to run on a low-power embedded device with a touchscreen, possibly on a remote, plug-in terminal to ensure system safety. While EPICS is planned as the system of choice for data transport and system monitoring, minimizing power means using EPICS in a different environment from its normal use case with always-on devices.

Long-term plans consist of using standard technologies that can be Ethernet-controlled (e.g. PoE) to allow for minimizing the use of custom components. This includes the desire to minimize cost by utilizing off-the-shelf RF-SoC devices that support robust power management schemes to minimize engineering and design effort.



Prototype architecture for LLRF



Prototype GUI for embedded controls

References

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