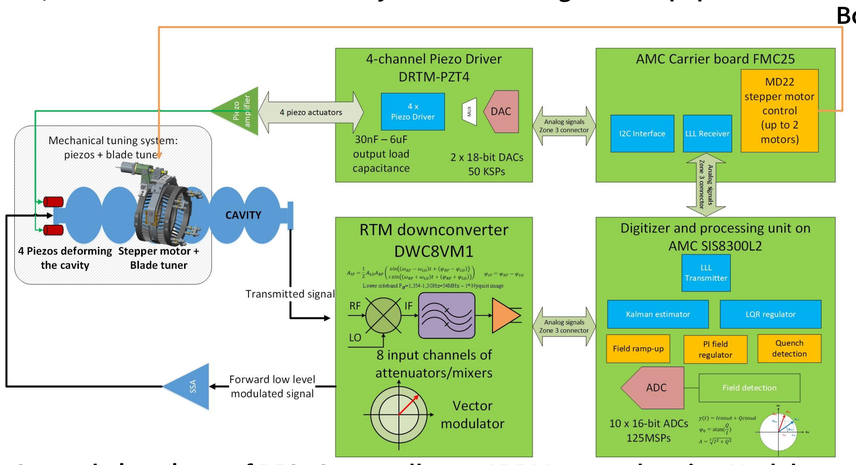
MEASURING AND CONTROL EQUIPMENT ON THE RFSOC FOR HOBICAT FACILITY

A. Ushakov†, A. Neumann, P. Echevarria, Helmholtz-Zentrum Berlin, Berlin, Germany

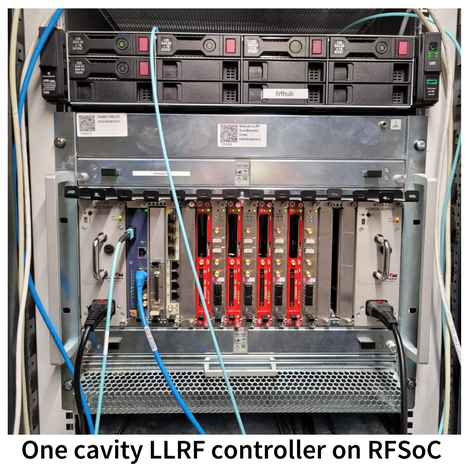
ABSTRACT: Controlling SRF cavities in CW mode in the presence of mechanical disturbances, as well as in the presence of noisy detectors, makes control still a challenge. Internal cavity features such as Lorentzian forces are well understood and predictable, but also make control difficult. An inexpensive solution for compact accelerators that can accommodate many algorithms simultaneously on a single board at an affordable price is RFSoC. Their analog circuits are not yet accurate. Nevertheless, a significant reduction in development time can be achieved through an integrated architecture, as well as development tools available on the market. The following will present the RFSoC control hardware with a focus on basic functions, implemented primarily as a firmware solution. The scope of functions is as follows: VNA measurements to determine resonator quality factor and S-parameters, PLL, control in the presence of noisy detector data, and adaptive RF/piezo control. The results of their tests on the Hobicat test facility will be shown.

CURRENT CONTROL SOLUTIONS IN SEALAB and HOBICAT FACILITIES

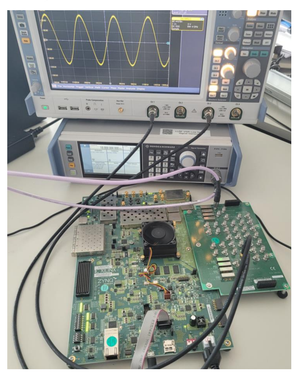
HW/FW Structure of the SRF Cavity controller using mTCA equipment



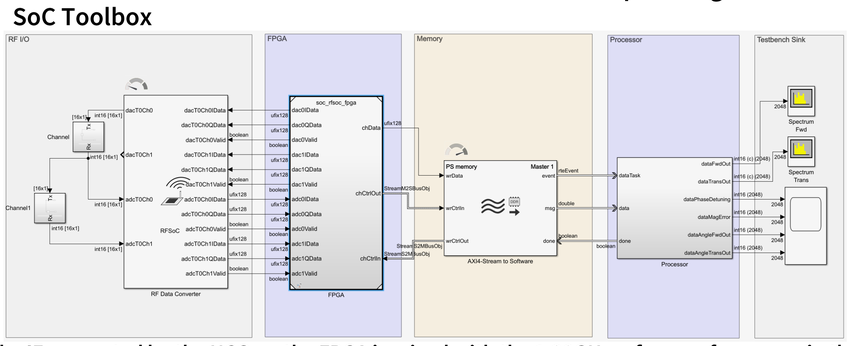
Sealab RFSoC Testing stand control of Gun and Booster



One cavity LLRF controller on RFSoC



General structure of RFSoC controller on ADPLL example using Matlab SoC Toolbox



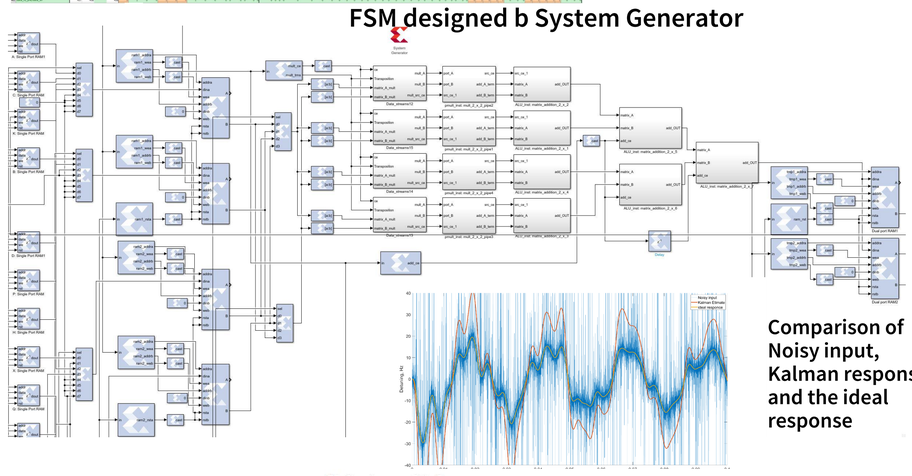
The IF generated by the NCO on the FPGA is mixed with the 1.28GHz reference frequency in the DAC so that the signal sent to the resonator is controlled by the first harmonic in the bandwidth of the resonator itself

STATUS OF KALMAN OBSERVER ON RFSOC

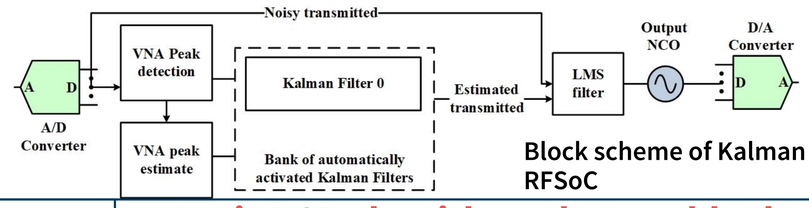
FSM controlling FPGA DSP resources usage

- FSM for the Kalman Filter was designed to track up to 20 mechanical modes.
- Optimization of the FPGA DSP resources was performed.
- The final accuracy of the observer is proportional to the number of modes in spite of the optimized sampling of the characteristic matrices
- It was decided not to use a single matrix to describe the state-space model, but to observe each excitation separately.

FSM designed b System Generator

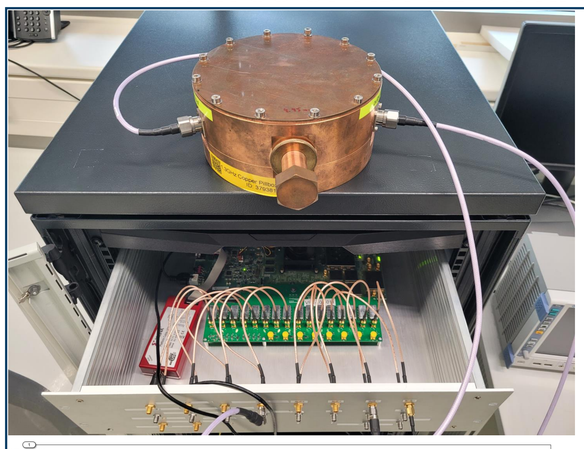


Comparison of Noisy input, Kalman response, and the ideal response



Block scheme of Kalman on RFSoC

STATUS OF ADPLL ON RFSoC



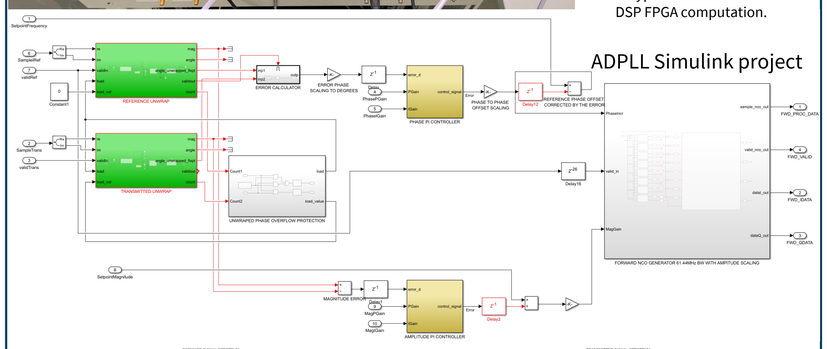
The main components of the ADPLL system:

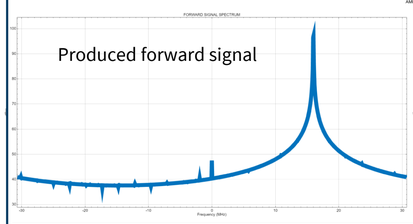
- The system reference frequency, i.e., the PLL output, is 7.68 MHz
- ADC/DAC sampling frequency is 3932.16 MHz
- Interpolation mode - 8, samples per clock - 8
- FPGA processing clock frequency is 61.44 MHz

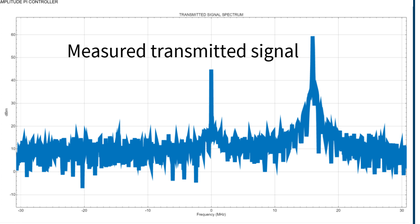
The main elements of the DSP, providing the operation of the algorithm, are:

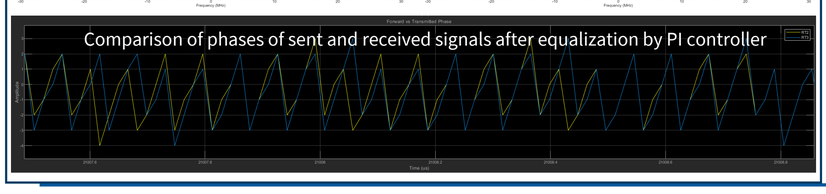
- Phase sweep calculator with overflow control;
- Multi-channel NCO generator with phase shift and increment;
- PI controllers for phase and amplitude correction;
- Polyphase FIR filter to enable DSP FPGA computation.

ADPLL Simulink project



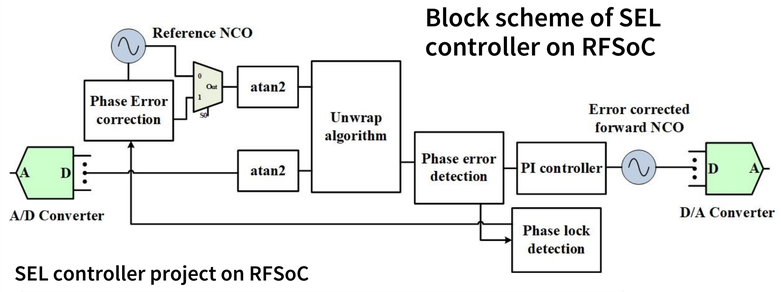




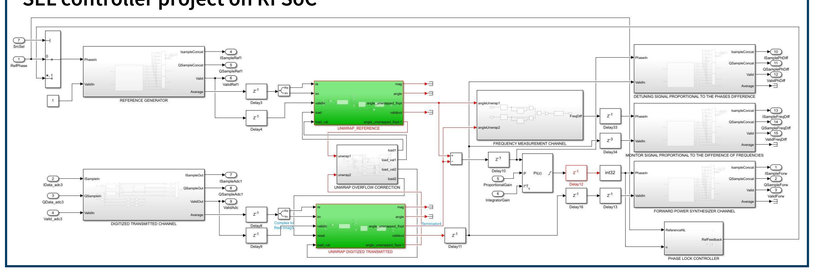


STATUS OF SEL ON RFSoC

Block scheme of SEL controller on RFSoC

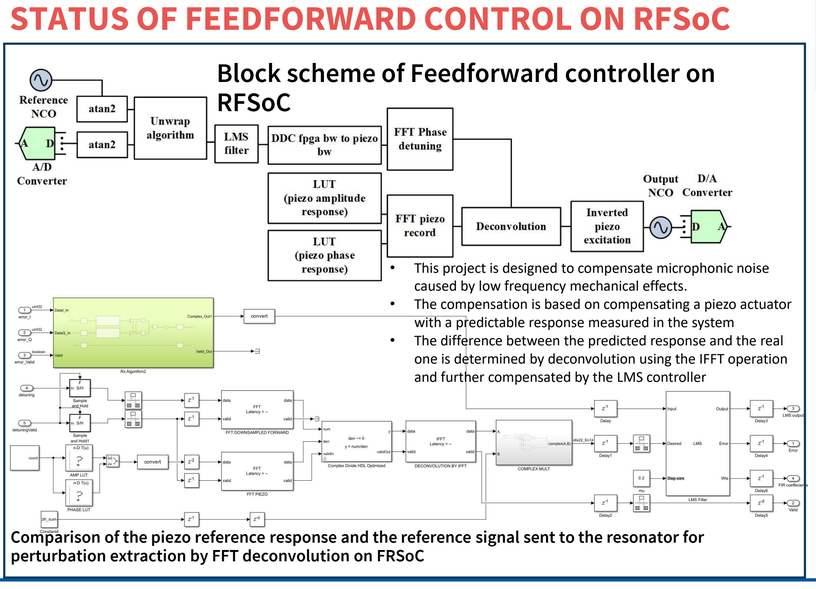


SEL controller project on RFSoC



STATUS OF FEEDFORWARD CONTROL ON RFSoC

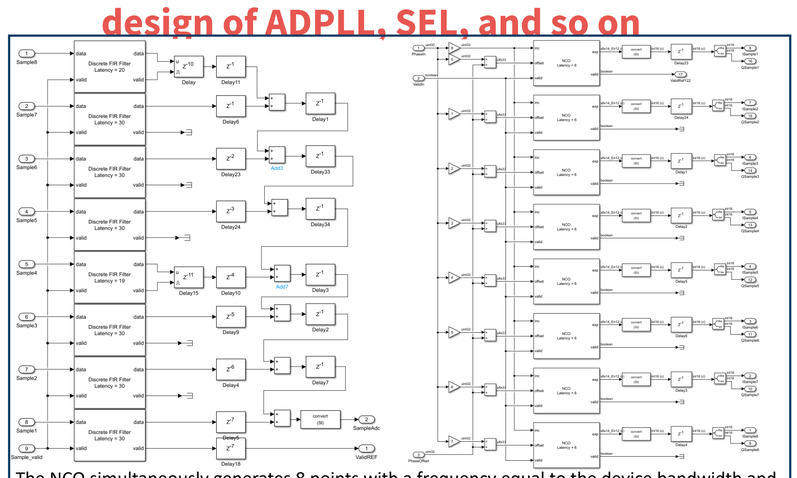
Block scheme of Feedforward controller on RFSoC



- This project is designed to compensate microphonic noise caused by low frequency mechanical effects.
- The compensation is based on compensating a piezo actuator with a predictable response measured in the system
- The difference between the predicted response and the real one is determined by deconvolution using the IFFT operation and further compensated by the LMS controller

Comparison of the piezo reference response and the reference signal sent to the resonator for perturbation extraction by FFT deconvolution on FRSoC

Basic DSP algorithms that enable the design of ADPLL, SEL, and so on



The NCO simultaneously generates 8 points with a frequency equal to the device bandwidth and simultaneously to the FPGA frequency, which will then be interpolated with a factor of 8. Thus the high-speed ADC/DAC is capable of digitizing/generating signals at a frequency close to the RFSoC frequency limit (about 4GSPS).
Simultaneous processing of 8 data points within the FPGA is possible by means of a polyphase filter

- RFSoC is a competitive control and instrumentation solution for laboratories with limited developer resources.
- Despite the relatively small market, the RFSoC is already significantly supported by both low-level and high-level development tools from both chip manufacturers and third-party developers.
- Tests on the Tesla resonator have already begun.
- Soon the algorithms will be provided with means for visualization and continuous recording of digitalized data of analog channels on the control computer.

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MORE INFORMATION

Dr. Andriy Ushakov

Andrey.Ushakov@helmholtz-berlin.de
Fon +49-30-8062-14993
the person in charge of the LLRF group of the SeaLab project,
Helmholtz Zentrum Berlin

Helmholtz Zentrum Berlin:
Dr. Pablo Echevarria, Dr. Axel Neumann