Digital LLRF system for SESRI Proton & Heavy Ion Accelerator Complex Injector

Ruifeng Zhang, Zhe Xu, Yan Cong, Shilong Li, Xiaodong Han, Ruihuai Zhou

Abstract

A 300 MeV proton and heavy ion accelerator complex has been designed and constructed by the Institute of Modern Physics for the space environment simulation and research infrastructure (SESRI) project. The linac injector of the accelerator complex is based on normal-conducting rf structures. It consists of an RFQ, a buncher, three DTLs, and two debunchers. The requirements for the rf field stabilities are ±1% in amplitude and ±1° in phase during flat-top. To satisfy these requirements, we developed a 108.48 MHz digital low-level RF system based on FPGA and compact PCI bus. This poster will present the design, implementation, and performance test.

Facility Layout

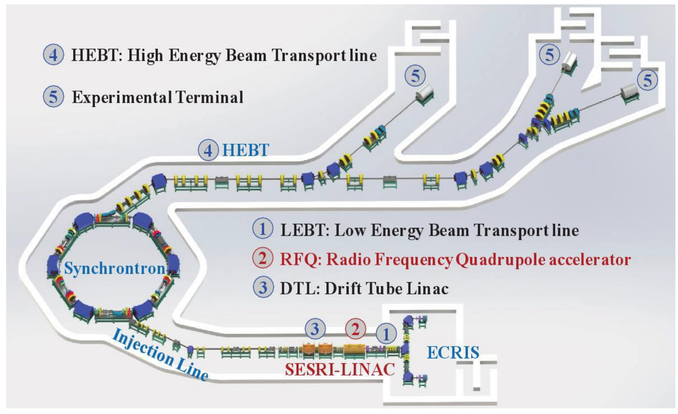
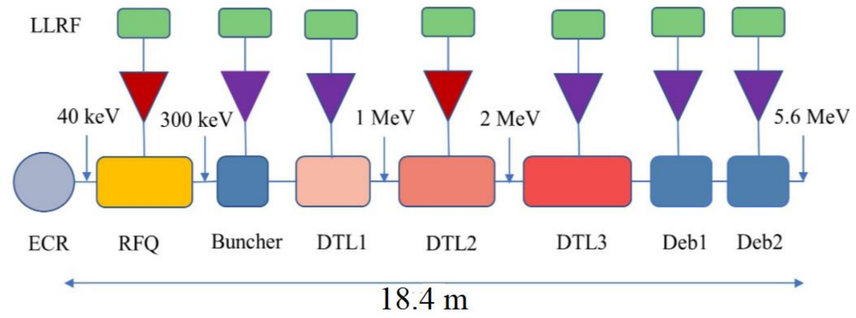


Table 1. Main parameters of the Facility

Ions	Energy(MeV)	Intensity(ppp)
p	300	1×10^9
$^4He^{2+}$	80	1×10^7
$^{84}Kr^{18+}$	15	1×10^7
$^{209}Bi^{32+}$	7	1×10^6

Linac Injector

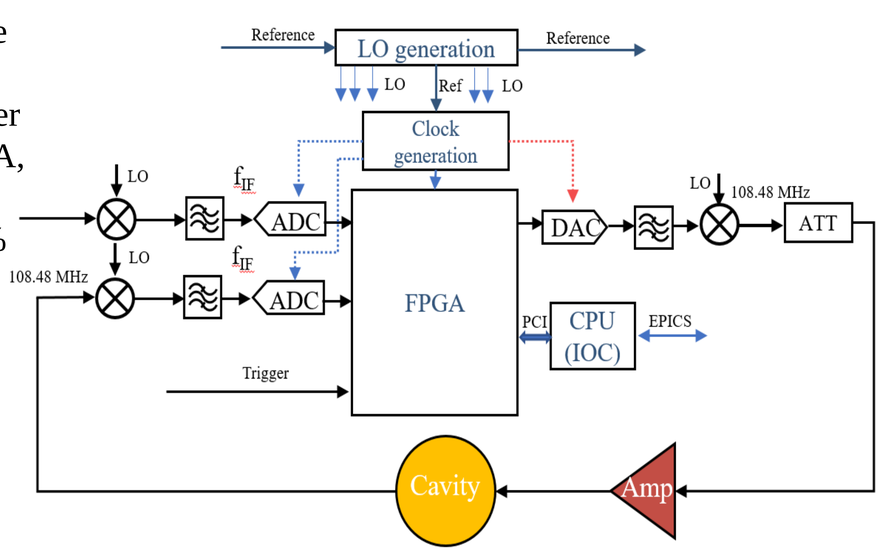


- 108.48MHz， pulse width ≤ 1ms，10Hz
- Stability requirement：±1%， ±1°
- Heavy ion beams， He^{2+}, Kr^{18+} and Bi^{32+} are accelerated by RFQ, DTL1, and DTL2 to 2 MeV/u
- H^{2+} beam is accelerated by RFQ, DTL1, and DTL2 to 2 MeV/u, then stripped into protons and further accelerated by DTL3 to 5.6 MeV.

LLRF Overview

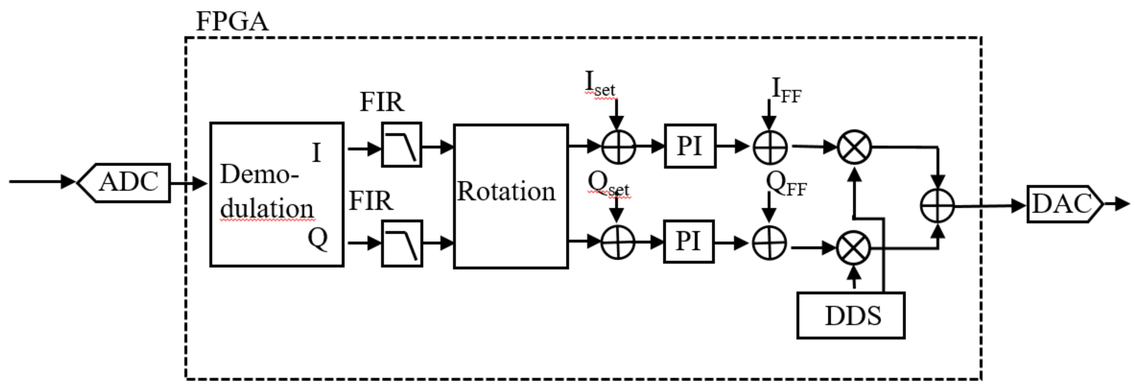
The digital low-level controller is based on high-performance ADC, DAC, and FPGA. It combines with the commercial standard CPCI chassis, supporting direct RF sampling and generation.

- High dynamic range (A/q=1…7)
- Non-linear amplifier characteristics (SSA, Tetrode)
- Amplitude ＜±1%
- Phase ＜±1°
- Fast interlock
- EPICS support
- Flexible clock configuration



Digital Signal Process

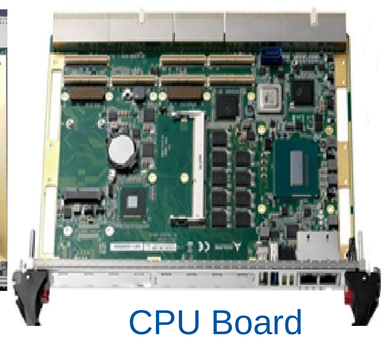
The 108.48 MHz rf signals from the cavity side are down converted to approximately 27.12 MHz intermediate frequency (IF) signals. The IF signals are sampled at 108.48 MHz , and then are fed to FPGA to perform digital signal processing .



Hardware

- 14 bit, 250 MSPS, ADC, LVDS
- 16bit, 1230 MSPS DAC, LVDS
- Xilinx V5 FPGA
- Configurable clock generation
- Commercial CPCI chassis and CPU board
- Microsoft windows 10 OS

FPGA Board



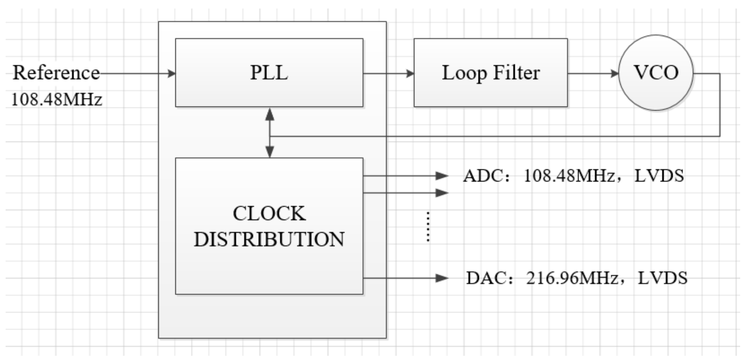
CPU Board

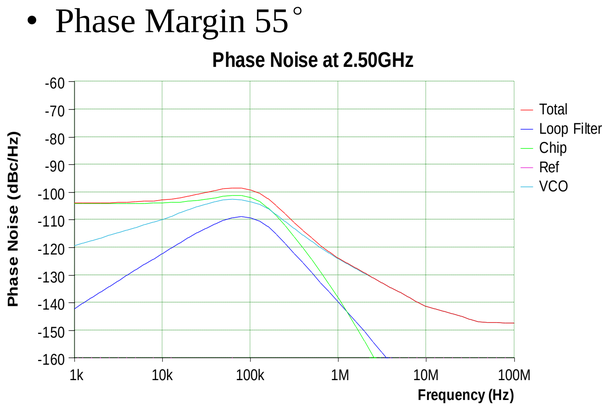
CPCI chassis

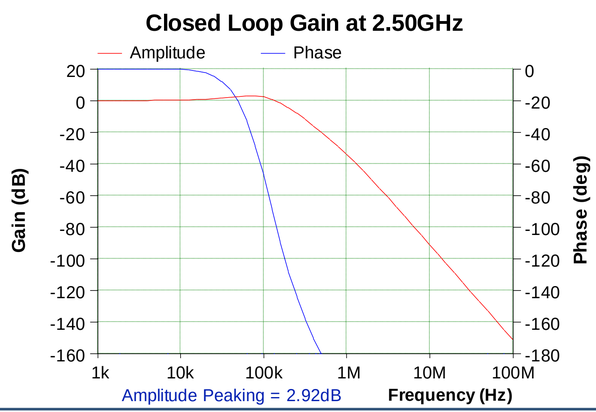
Clock Generation

AD9516-1 Clock Distribution

- Integrated PLL
- Integrated VCO 2300MHz - 2650MHz
- 4 LVDS or 8 CMOS
- Configure by SPI bus
- Loop Bandwidth 100kHz
- Phase Margin 55°

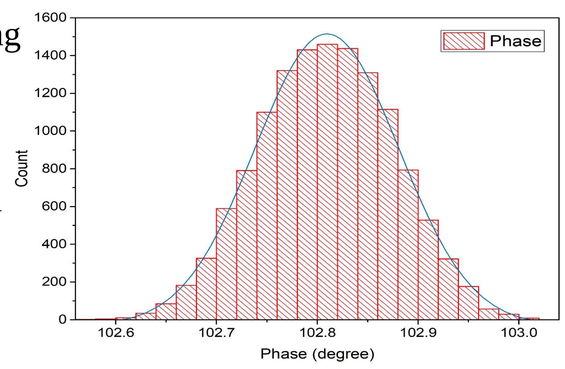


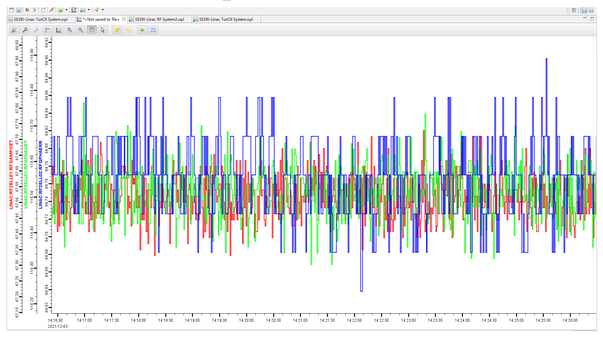




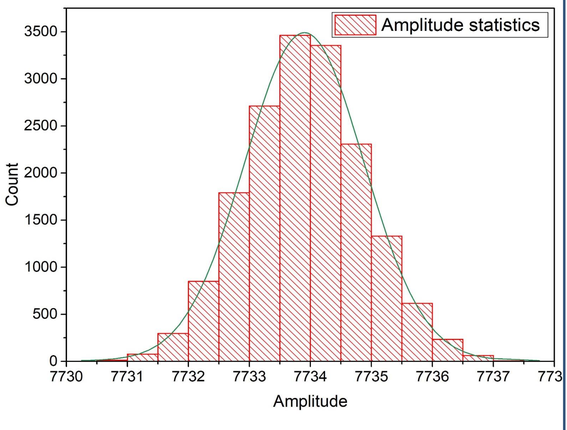
Conclusion

- Digtial LLRF system based on IF ampling & IF up-conversion using IQ control method
- Stability of <**±0.2%,±0.2deg.** is obtained during rf pulse with a Buncher1 test
- 8 hours long stability of ±0.28%，±0.22deg with a RFQ test
- Direct RF sampling and A&P control is under develop



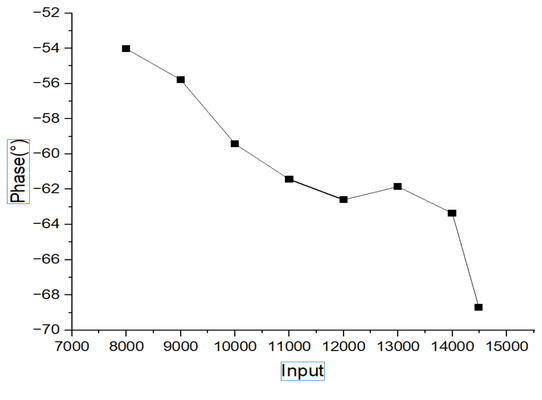


A/q = 6.5, power 107 kW，amplitude：±0.28%；phase： 0.44°

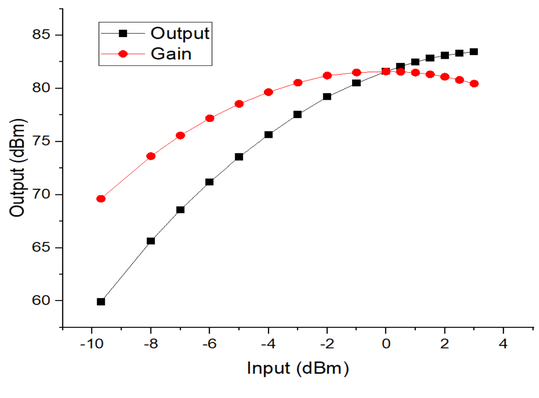


SSA nonlinearity

- Two 150 kW solid state amplifier used for DTL1 & DTL3 separately.
- AM-PM distortion.



- AM-AM distortion



Poster ID：55

LLRF2023 LOW LEVEL RADIO FREQUENCY WORKSHOP 2023 OCTOBER 22-27, 2023 IN GYEONGJU, REPUBLIC OF KOREA

Institute of Modern Physics, CAS
Add：No.509 Nanchang Road Lanzhou, China
Email: zhangruifeng@impcas.ac.cn