Status of the PEG in-kind contribution to the ESS LLRF systems integration and installation

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Abstract

The Polish Electronic Group (PEG) is currently in the final stage of the Polish in-kind project realization. This endeavor is dedicated to the chosen modules of LLRF system design and production, LLRF system integration, and installation in the dedicated ESS accelerator infrastructure. This contribution describes the latest achievements in the LLRF system integration and installation for the M-Beta and H-Beta sections. The status and plans for the final production of MTCA.4 modules like Piezo RTM driver, LO RTM, RTM carrier AMC card are discussed as well.

Polish Electronic Group

Polish Electronic Group (PEG) - Polish *in-kind* to EES

- National Centre for Nuclear Research (NCBJ) (leader),
- Warsaw University of Technology (WUT)
- Technical University of Lodz (TUL).

LLRF systems for ESS elliptical resonators

ESS LLRF systems

- single cavity regulation scheme,
- modular design thanks to MTCA.4 standard - unified approach for all resonator types,
- prepared for 352 MHz and 704 MHz proton accelerator systems,
- comprises from COTS and PEG modules (RTM Carrier, LO-RTM, Piezo Driver RTM),
- integrated with E3 - EPICS control system.

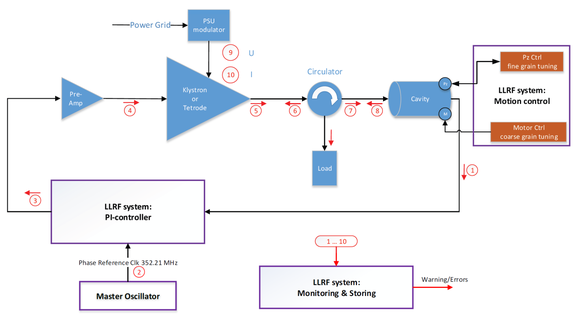

Figure 1: Overview of the LLRF system control loop

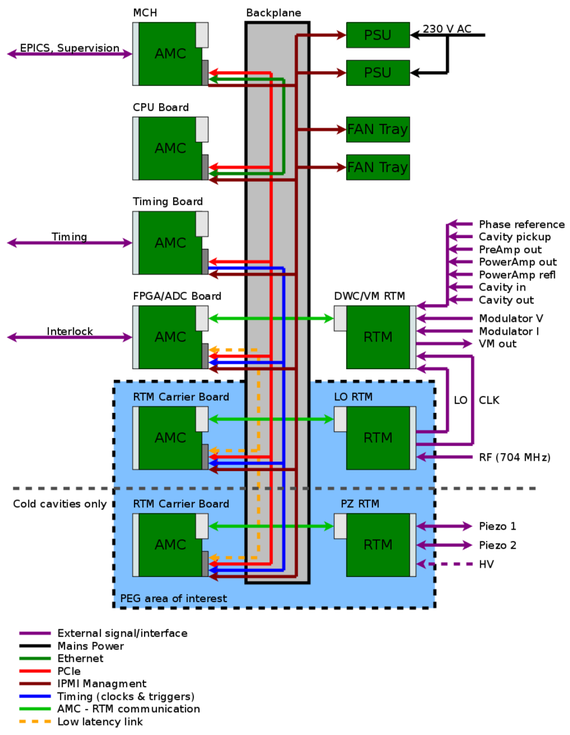

Figure 2: Layout of the MTCA.4 based LLRF system

Cavity Simulator

- designed to help in LLRF system development and verification,
- suitable for the elliptical (M- and H- beta) cavities models,
- includes cavity dynamics, piezo detuning, beam current and amplifiers nonlinearities,
- under operation at PEG partners and the ESS side,
- comprises of the high-performance FPGA, data converters modules and dedicated RF frontend.

Figure 3: Cavity Simulator front panel

LLRF test stand

- mimics behavior of the LLRF control loop - the single RF cell,
- allows for close loop operation without costly cryomodule infrastructure,
- comprises of the LLRF systems (with PEG delivered modules) and cavity simulator,
- independent, stand alone, complete loop setup,
- used by PEG for:
  - integration tests scope and software preparation and validation,
  - PEG HW modules firmware and low level software development and verification,
  - integrated LLRF system components hardware and software troubleshooting,
  - higher level software applications development and testing.

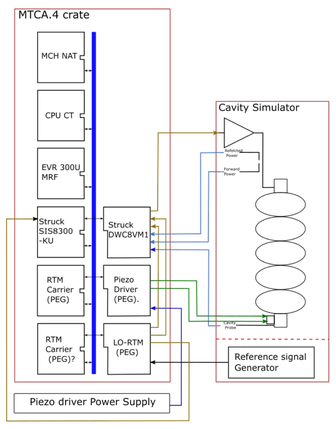

Figure 4: LLRF test stand layout

ACKNOWLEDGEMENTS

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MTCA.4 hardware modules designed, delivered and integrated by PEG

- Purpose: simple, low cost FPGA based MTCA.4 AMC; supporting LO RTM and Piezo RTM modules
- Technical data: Artix-7 FPGA ; 1GB of DDR3 memory; PCIe x2 ; Low latency Links on the AMC backplane
- Status:
  - mass production for M-Beta system completed,
  - M-Beta installation in the LLRF systems - completed,
  - H-Beta production in progress.

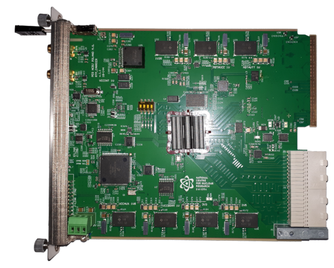

Figure 5: RTM Carrier AMC board

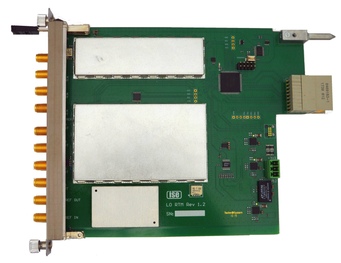

Figure 6: LO RTM Revision 1.2

- Purpose: generate and distribute clock and Local Oscillator sig. for 4 LLRF systems,
- Technical data:
  - clock - $f_{ref}/6 = 117.403$ MHz,
  - LO - $f_{ref} * 23/22 = 736.439$ MHz or $f_{ref} * 29/28 = 729.578$ MHz
  - Reference frequency = 704.42MHz
- Status:
  - mass production for M-Beta - completed,
  - design adjustments and mass production for H-Beta - completed,
  - installation in the LLRF systems - done (for M-Beta and H-Beta completed in the gallery).

- Purpose: Piezo tuners control and monitoring signal acquisition,
- Technical data:
  - 2 channels for piezo actuator/sensor mode operation,
  - unipolar/bipolar/asymetric mode of operation possible within -200V to 200V range and 3 kHz bandwidth,
  - external 19" HV power supply module with remote diagnostic,
- Status:
  - system design adapted to the device operation specification change and due to the semiconductor crysis,
  - RTM modules and power supply mass production completed for M- and H-Beta systems
  - M-Beta, H-Beta and Spoke cavities installation completed,
  - post-installation testing and evaluation in progress.

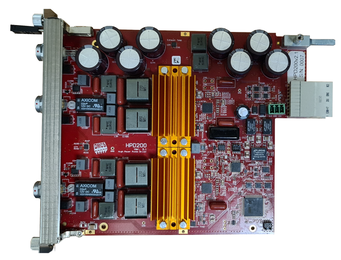

Figure 7: Piezo Driver RTM ver. 2.1 (final prototype)

Other hardware modules

PSS switch

- blocks LLRF system output in case of emergency,
- controlled by Personal Safety System,
- based on the RF relay (by Radial),
- all modules produced, tested and delivered to ESS.

Figure 8: PSS Switch

Figure 9: PIN-diode

PIN diode

- fast RF gate that blocks LLRF system output,
- controlled by the MPS (Machine Protection System),
- design with the MPS health status verification option,
- most modules produced, tested and delivered to ESS.

Electron Pick-up

- protection system - measures current from the multipacting,
- activates interlock if threshold exceeded - sends info to the MPS system,
- form factor unified with PIN diode,
- most modules produced, tested and delivered to ESS.

Figure 10: Electron Pick-up

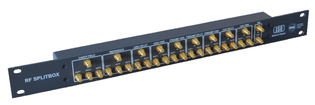

Figure 11: RF SpiltBox

RF SplitBox devices:

- RF signal distribution inside the LLRF racks,
- consists of 9 custom-designed power splitters optimized to archive the lowest possible phase drifts,
- optimized for very low crosstalk,
- different versions for different parts of the linac - production completed.

Systems integration and installation

- Testing and installation: MTCA.4 crate post assembly test with Cavity simulator (Factory Acceptance Test), installation in the klystron gallery, inner rack cabling, second test run in final destination (SAT),
- Prepared standalone portable testing environment - with stable software versions,
- all LLRF Medium Beta systems installed,
- the LLRF systems for H-Beta installation in progress (up to the quantity required for "beam on target"),
- installation will be completed by Q1.2024.