Progress in LLRF system development for Korea-4GSR

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Oct. 24, 2023

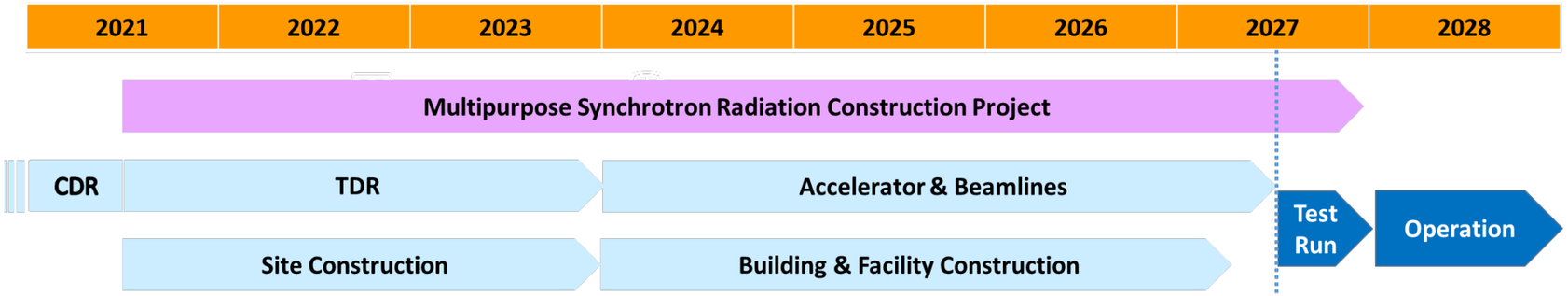
4GSR project background

- **Multipurpose Synchrotron Radiation Construction Project**
  - Period: 2021 July to 2027 June (6yrs)
  - Budget: 1.0454 Trillion KRW (≈ USD 750M)
  - Land: 540,000 ㎡ / Building: 69,400 ㎡
  - Location: Ochang, Chungcheongbuk-do

4GSR Project Budget Plan **(Million USD)**

Years	2021	2022	2023	2024	2025	2026	2027	Sum
Machine	8	44	77	172	180	97	28	606
Site	72	72	-	-	-	-	-	144
Sum	80	116	77	172	180	97	28	750

- **Project Timeline**



Korea 4GSR

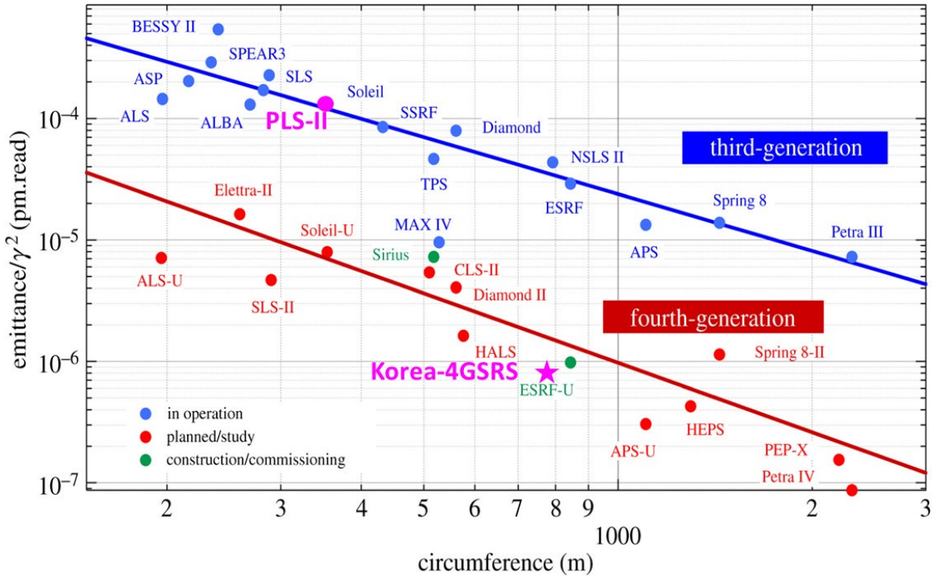
4GSR project background

- **Specifications**
  - Korea-4GSR is to be a 4th generation storage ring based light source
  - The beam energy of this facility is 4 GeV, and the beam emittance is 58 pm rad with the beam current of 400 mA.
  - 4GSR aims to reduce the emittance by more than 100 times compared to 3GSR by further increasing the number of dipole magnets installed in one storage ring cell.

Comparison of parameters of PLS-II and 4GSR

Parameter	Values		Unit
	PLS-II	4GSR	
Beam energy	3	4	GeV
Beam average current	400	400	mA
Straight sections - No.	12	28	-
Straight sections - length	3.7 / 6.8 long	6.5	m
Ring circumference	281.8	798.8	m
Emittance	5,800	58	pm rad
Harmonic number	470	1332	-
Bunch length (ps) (with H.C)	20	53.4	ps
Injection	Full energy Linac	Booster Ring	-

Emittance vs Circumference

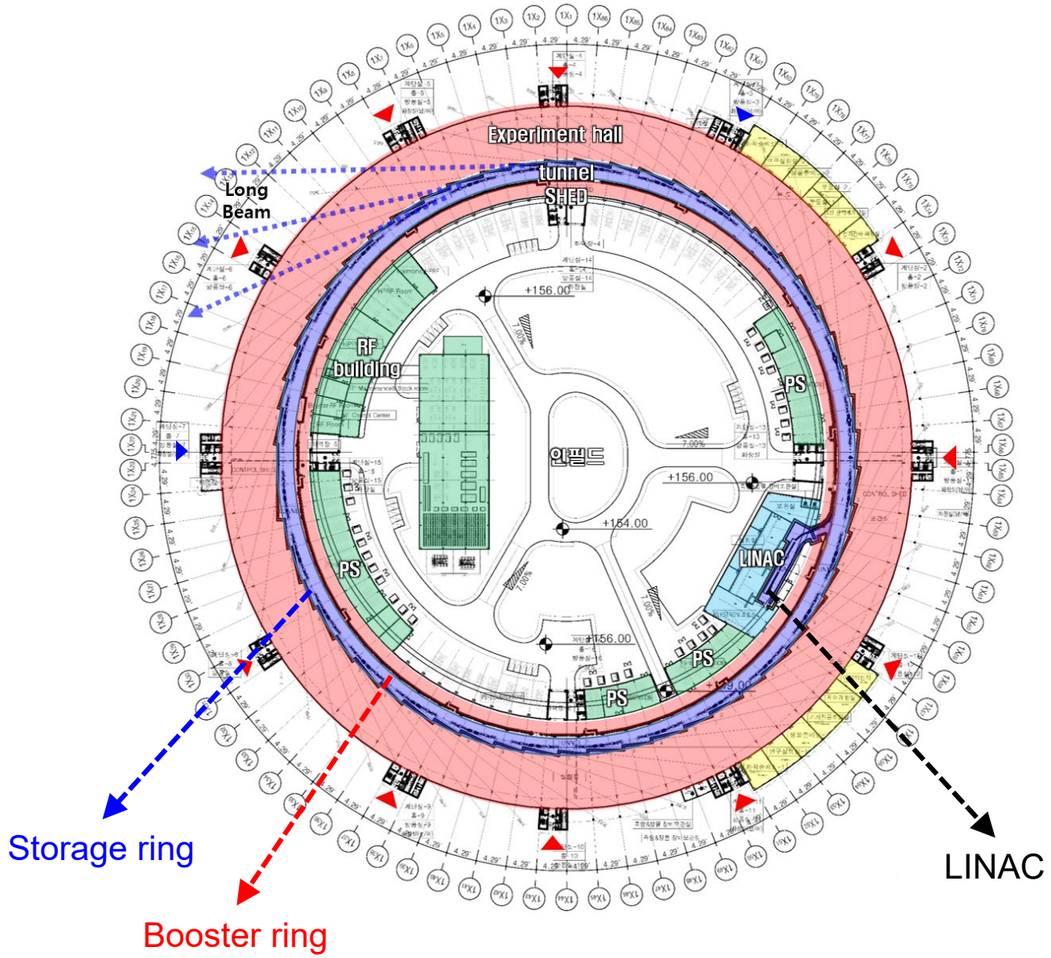


4GSR project background

- The project structure combines the two entities of Pohang Accelerator Laboratory (PAL) as well es Korea Basic Science Institute (KBSI).
- Exclusive charge taskforce inaugurated for the success of the project → PAL expert's participation for construction of accelerator and beamline

Affiliation	Specialty	Job share rate (%)	Remark
PAL - 1	RF physics	30	Storage ring
PAL - 2	LLRF & RF Control	30	Storage ring
PAL - 3	Automation & Diagnosis	30	Storage ring
PAL - 4	System integration, Layout	30	Storage ring
PAL - 5	HPRF & Transmission	30	Storage ring
PAL - 6	Cooling & Vacuum	30	Storage ring
4GSR	Cavity & RF physics	100	Storage ring & booster
4GSR	System integration	100	Storage ring & booster

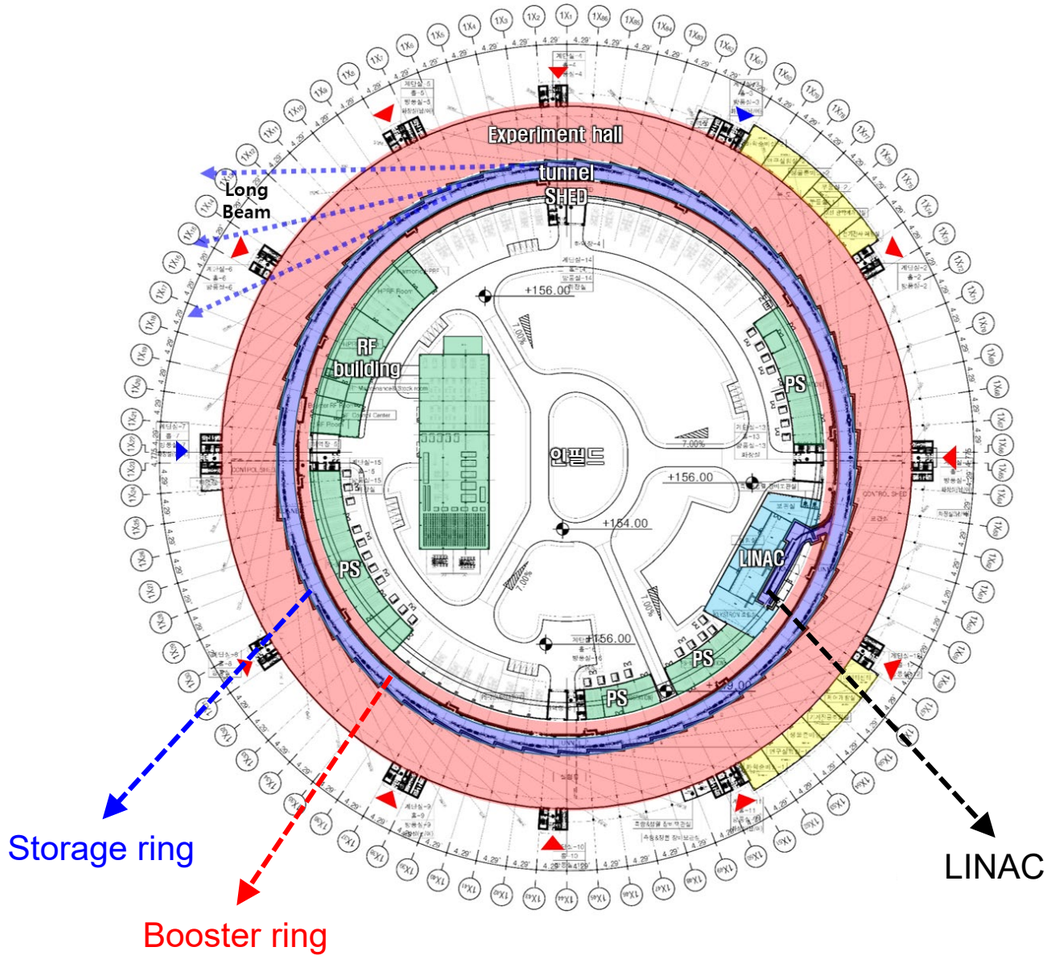
Overview of RF parameter (Storage ring)



RF parameters for storage ring

Parameter	Values
RF frequency [MHz]	499.593469
Energy [GeV]	4.0
Current [mA]	400
Circumference [m]	799.297
Revolution frequency [MHz]	3.7507
Harmonic number	1332
Electron energy loss/turn (KeV)	1877.65
Beam loss power by synchrotron radiation [kW]	751.06
Accelerating Voltage [MV]	3.5

Overview of RF parameter (Booster ring)



RF parameters for Booster ring

Parameter	Values
RF frequency [MHz]	499.594
Energy [GeV]	0.2 - 4.0
Current (single/multi) [mA]	1 / 3
Circumference [m]	0.3
Revolution frequency [MHz]	387.9
Harmonic number	1288
repetition rate [Hz]	2
Energy loss per turn @ 4.0 GeV [MeV]	1.671
Accelerating Voltage @ 0.2 GeV [MV]	0.3
Accelerating Voltage @ 4.0 GeV [MV]	3.0

Choice of storage ring cavity

Cavities in other accelerators for storage ring

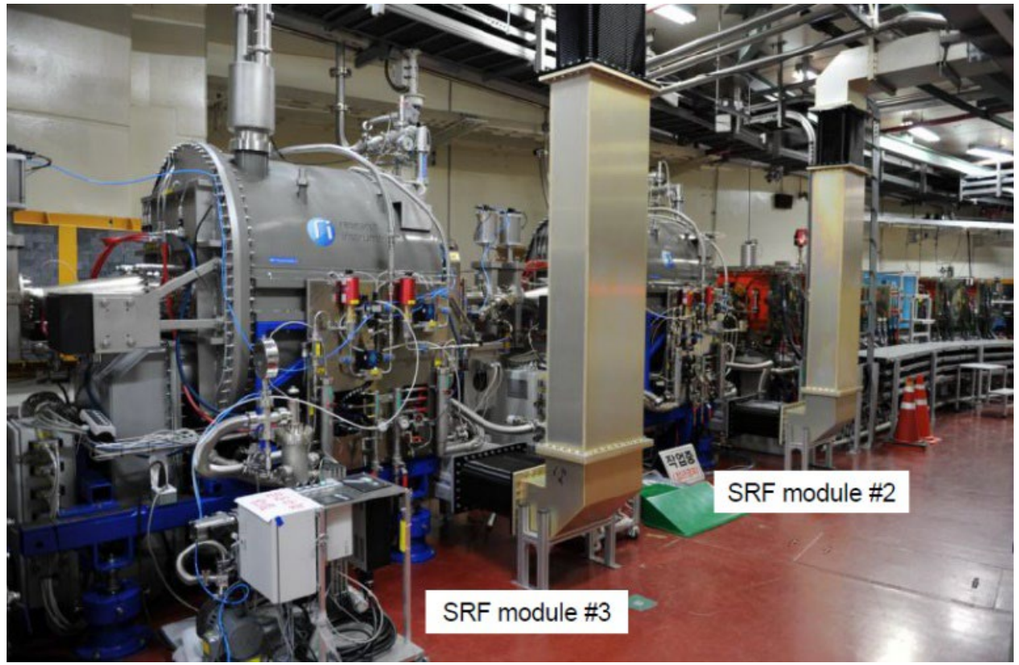
4th generation

Light Source	Cavity Type	Energy	Frequency	Circumference	Current	Cavity type (#)	RF power [kW]	Accelerating voltage (/cavity) [MV]	Energy loss/turn [MeV]
ESRF-EBS	**NC**	**6.0**	**352**	**844.4**	**200**	**EU-HOM (13)**	**79**	**6 (500 kV)**	**2.56**
APS-U	**NC**	**6.0**	**352**	**1104**	**200**	**EU-HOM (12)**	**82.7**	**5.53 (535 kV)**	**6.57**
PETRA-IV	**NC**	**6.0**	**500**	**2304**	**200**	**EU-HOM (24)**	**110**	**8 (333 kV)**	**4.02**
Diamond-II	**NC**	**3.5**	**500**	**561.6**	**300**	**EU-HOM (8)**	**73**	**2.7 (338 kV)**	
SLS-II	**NC**	**2.4**	**500**	**290**	**400**	**EU-HOM (3)**	**114.9**	**1.4 (450 kV)**	**0.688**
HEPS	SC	6.0	166	1295	200	SC (4)	150	3.5 (1200 kV)	2.5
NSLS-II	SC	3.0	500	158.4	400	SC (4)	270	4.8 (1200 kV)	~ 2.0
SIRIUS	SC	3.0	500	518.4	350	SC (2)	240	3.0 (1500 kV)	0.873 (bend & ID)
SSRF	SC	3.5	500	180	240	SC (3)	-	4.6 (1800 kV)	1.44
NSRRC	SC	3.0	500	496.8	300	SC (2)	440	3.2 (1600 kV)	1.58
ALBA	NC	3.0	500	400	400	NC (6)	150	3.6 (600 kV)	1.3

- 4th generation light source using the normal conducting, almost use the EU-HOM damped cavity model.

Choice of storage ring cavity (S.C vs N.C)

- Superconducting cavity has the advantages in respect to HOM characteristics.
- PLS-II has operated 3 superconducting cavity from 2011



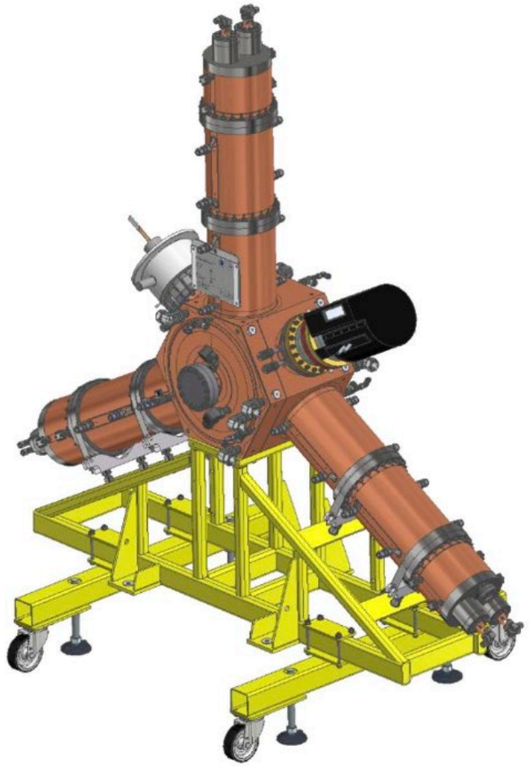
CESR-B SC cavity (PLS-II)

Normal cavity

- For the simpler operation, easier maintenance and reparability of cavity we have chosen a normal conducting cavity for 4GSR project

Cavity choice for storage ring

- 10 EU-HOM damped cavities for the storage ring to generate the total accelerating voltage of 3.5 MV and to compensate the beam energy loss



EU-HOM damped Cavity (RI)

Parameter	Values	Remark
Accelerating voltage [MV]	**3.5**	
Number of cavity	**10**	
Optimal Coupling beta	4.5	
Required accelerating voltage per cavity [MV/cav]	**0.35**	Correspond to 1.2 MV/m
Wall loss power per cavity [kW/cav]	18.01	
Beam loading power per cavity [kW/cav]	**75.11**	
Power loss at HOM absorber [kW/cav]	5	
Required power to coupler per cavity [kW/cav]	**98.57**	Max power of coupler : 120 kW
Transmission line loss per cavity [kW/cav]	10	circulator, waveguide, etc.
Required output power of HPRF [kW/cav]	**108.57**	
Rated power of HPRF [kW/cav]	**150**	abt. 73% of RF source rated power

Choice of booster ring cavity

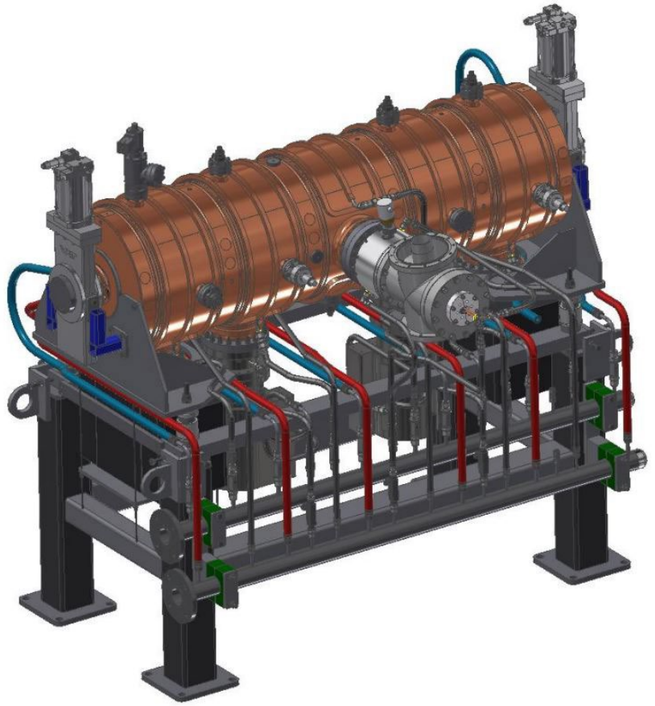
Cavities in other accelerators for storage ring

Light Source	Energy [GeV]	Freq. [MHz]	Circumference [m]	Rep. rate [Hz]	Cavity type (#)	Total Gap Voltage [MV]	Gap Voltage / Cavity [MV]
ESRF-EBS	0.20 → 6.0	352	298	4	5 cell LEP (4)	9.00	2.25
APS-U	0.45 → 6.0	352	368	2	5 cell LEP (4)	8.30	2.07
PETRA-IV	0.45 → 6.0	500	316.8	2 ~ 5	5 cell PETRA (9)	12.0	1.33
Diamond-II	0.10 → 3.5	500	163.8	5	5 cell PETRA (2)	2.00	1.00
SLS-II	0.10 → 2.4	500	270	3	ELETTRA (4)	2.60	0.65
HEPS	0.50 → 6.0	500	454	2	5 cell PETRA (6)	8.00	1.33
NSLS-II	0.20 → 3.0	500	158.4	1	7 cell PETRA (1)	1.20	1.20
SIRIUS	0.15 → 3.0	500	496.8	2	5 cell PETRA (1)	1.05	1.05
SSRF	0.10 → 3.5	500	180	2	5 cell PETRA (2)	1.74	0.87
TPS	0.15 → 3.0	500	496.8	3	5 cell PETRA (1)	1.20	1.20
BESSY-II	0.05 → 1.9	500	96	10	5 cell PETRA (1)	-	-
ALBA	0.10 → 3.0	500	249.6	3	5 cell PETRA (1)	1.00	1.00

- Multi-cell cavities are more efficient in reducing the footprint and cost than single-cell cavities, many accelerators multi-cells, especially 5-cell cavities, are used for booster ring.
- In the booster ring, the beam current is lower than that of storage rings, affect of HOM is not critical.

Cavity choice for Booster ring

- 5-cell normal conducting cavity of PETRA type has chosen in consideration of cost, space saving and field tuning.

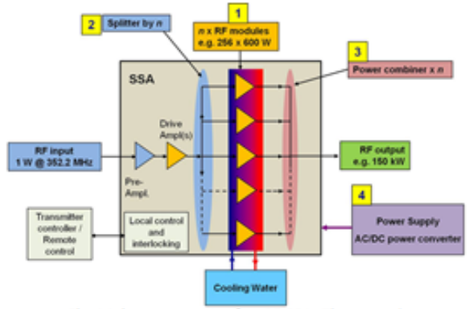


Petra-IV 5 cell cavity (RI)

Parameter	Values	Remark
Accelerating voltage [MV]	**3.5**	
Number of cavity	**3**	
Optimal Coupling beta	~ 1.02	
Required accelerating voltage per cavity [MV/cav]	**1.17**	
Wall loss power per cavity [kW/cav]	45.37	
Beam loading power per cavity [kW/cav]	**1.05**	
Required power to coupler per cavity [kW/cav]	**46.42**	
Transmission line loss per cavity [kW/cav]	9.6	circulator, waveguide, etc.
Required output power of HPRF [kW/cav]	**56.02**	
Rated power of HPRF [kW/cav]	**80**	abt. 70% of RF source rated power

High power RF system

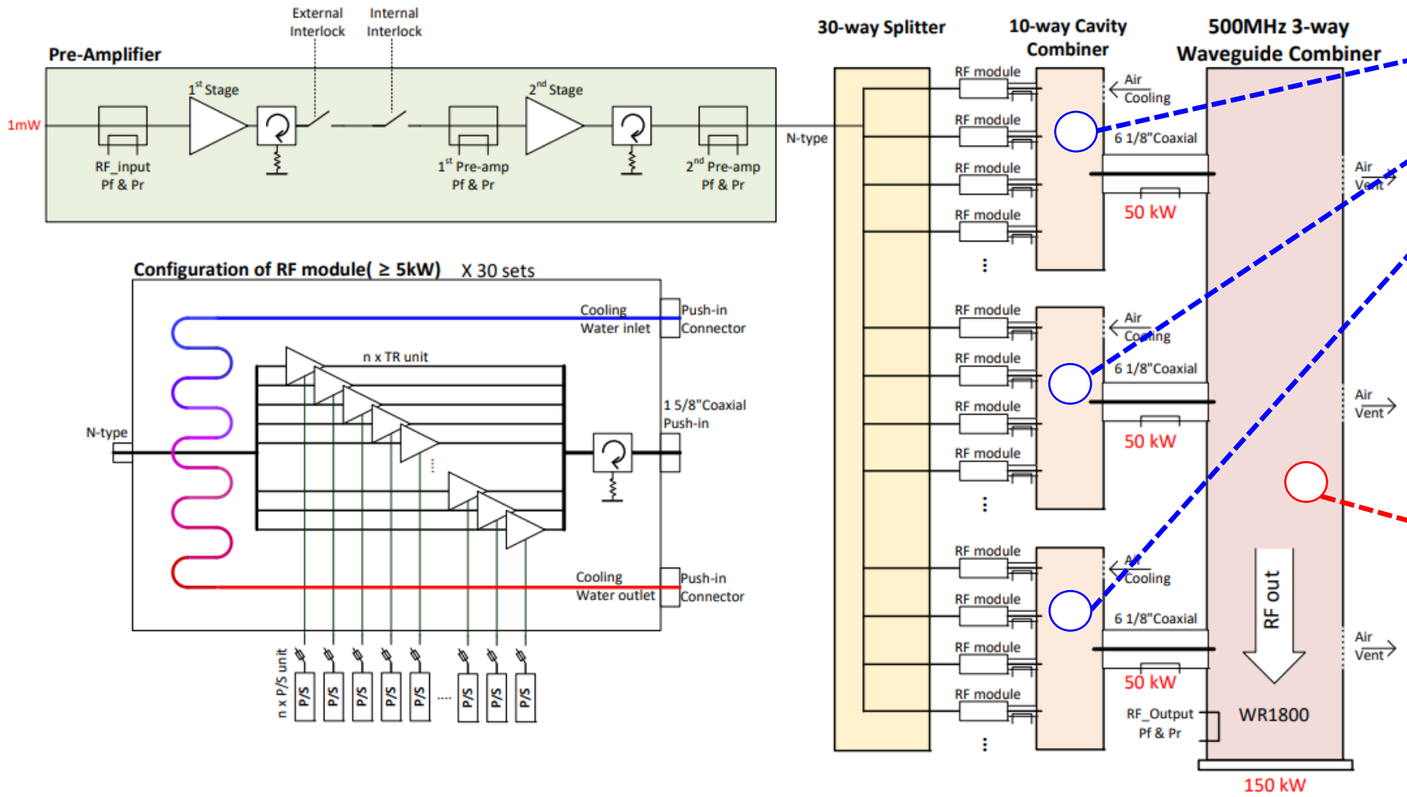
- Comparison between Klystron and SSPA Based on 150kW

Comparison	Klystron	SSPA(Solid State Power Amplifier)
	  Fig. 500 MHz, 300kW cw Klystron at Pohang Light Source –II	 Fig. Main components of an RF SSA. The example
Advantage	▪ ~~Less space~~ ▪ Long lifetime(>50,000hrs) ▪ Many references	▪ Lower price (Abt. 95% of Klystron) ▪ Higher operability (Operation with faults) ▪ Easy maintenance by modularity ▪ Lower phase noise(Abt. -68dBc) ▪ Easier to upgrade in future ▪ No additional shielding for High Voltage and X-ray required
Dis-advantage	▪ High price (increasing annually) ▪ Whole replacement is required at Fault ▪ Declining Industries ▪ High Voltage Protection required ▪ X-ray Shielding required ▪ PWM Ripple(Abt. -50dBc)	▪ ~~More space is required~~ ▪ Less references

Solid state amplifier

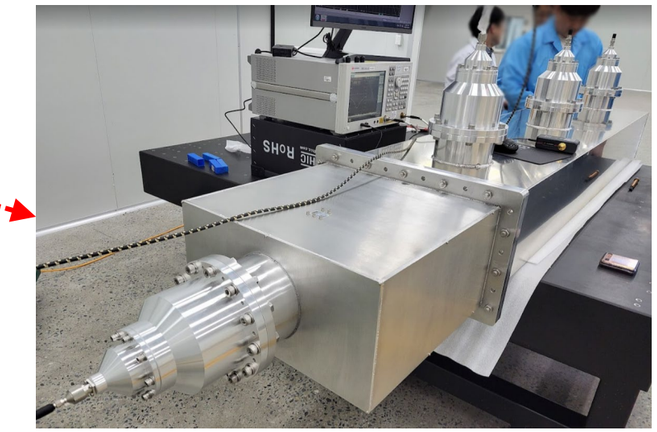
Exhibition booth : RFHIC

- 1st stage : 3 of 10 way cavity combiner (tested RL 42 dB)
- 2nd stage : 1 of 3 way WR1800 WG combiner (tested RL 39 dB)
- Final stage : Prototype 150kW SSPA package



Concept diagram of the 150 kW SSPA

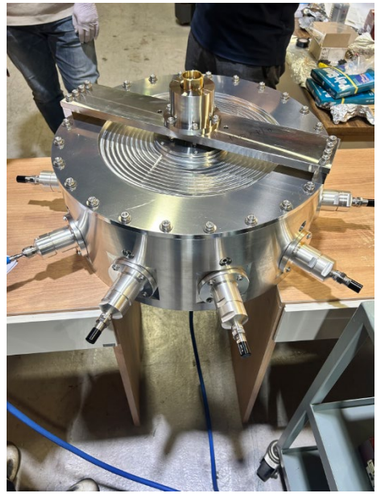
10 way cavity combiner for the SSPA

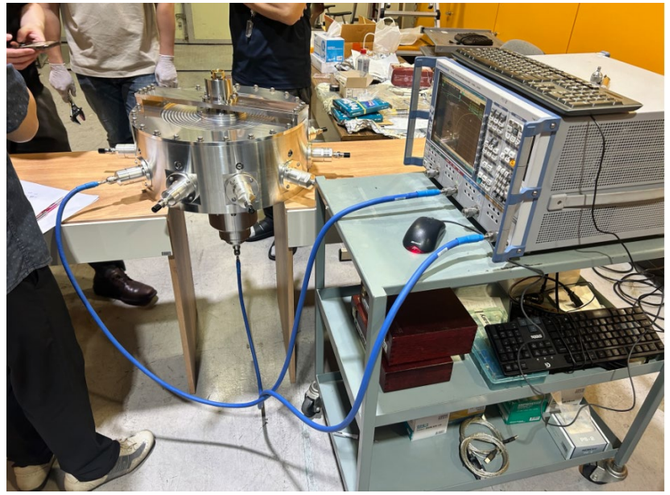


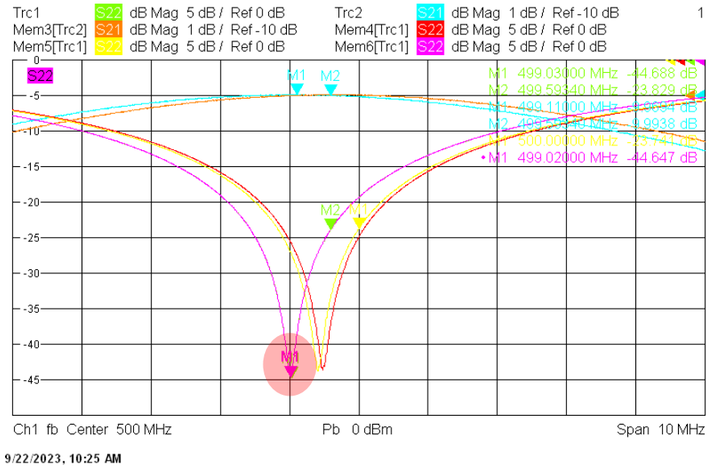
3 way WR1800 combiner for the SSPA

Solid state amplifier (10 way cavity combiner)

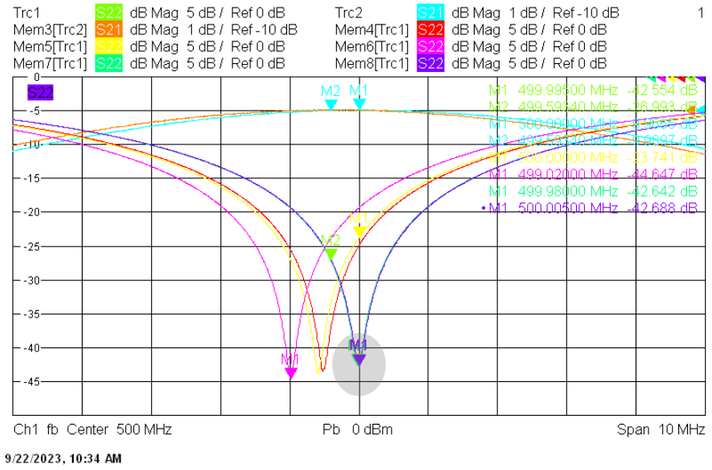
Exhibition booth : RFHIC



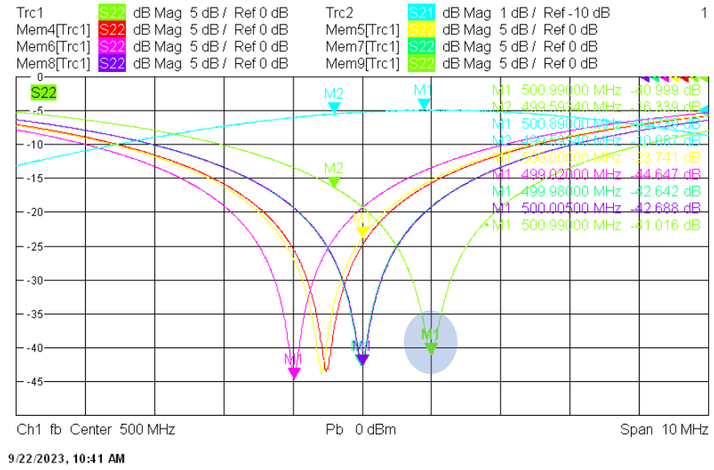




499.02 MHz / -44.647 dBm

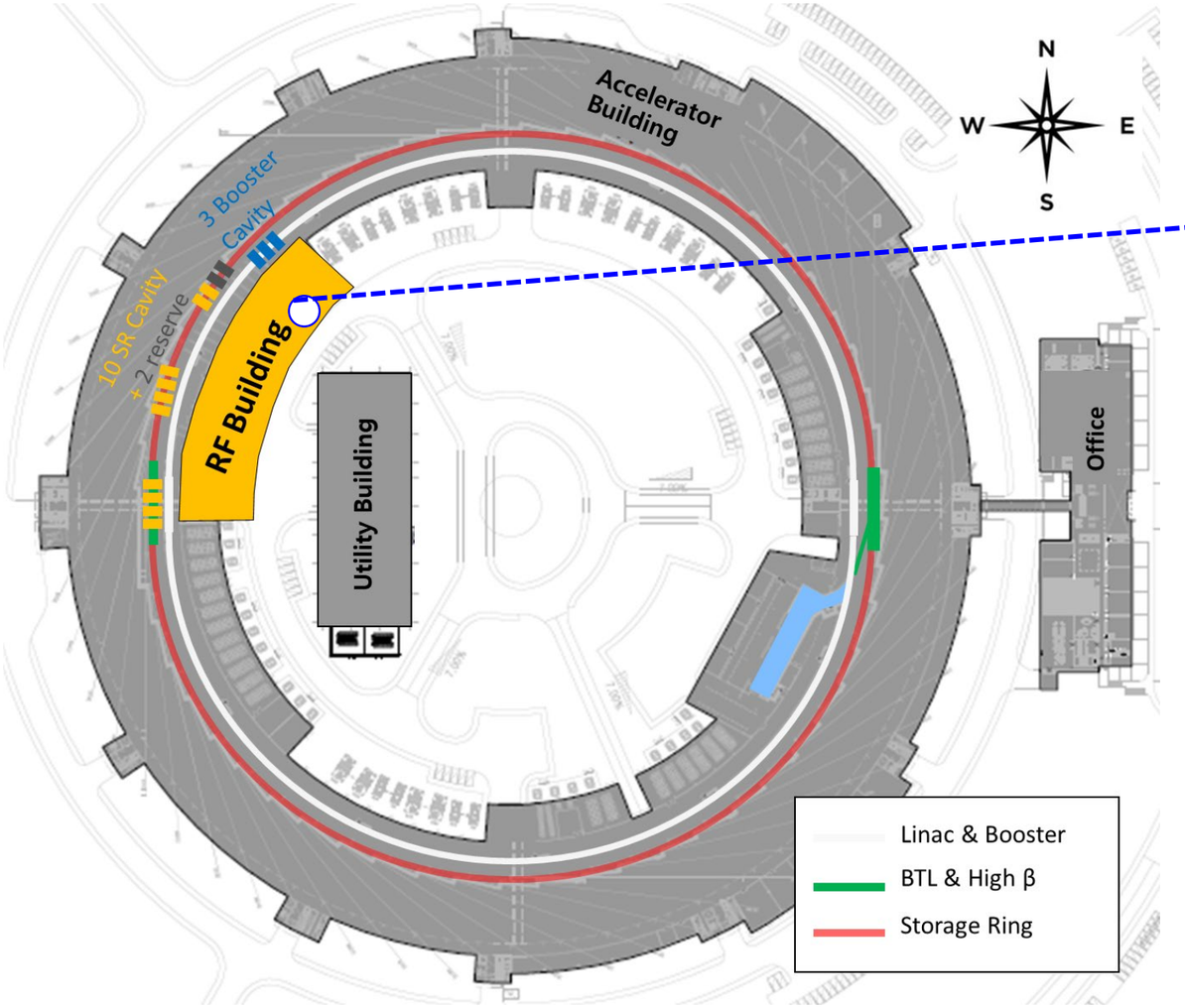


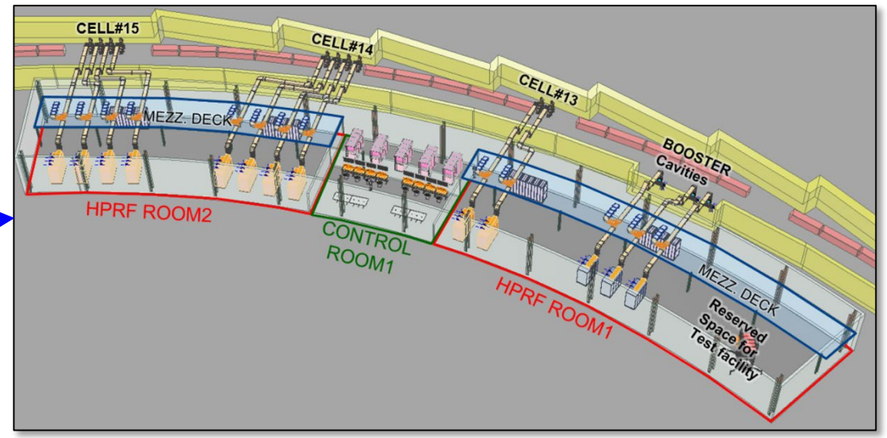
500.005 MHz / -42.688 dBm



500.99 MHz / -41.016 dBm

layout of 4GSR facility

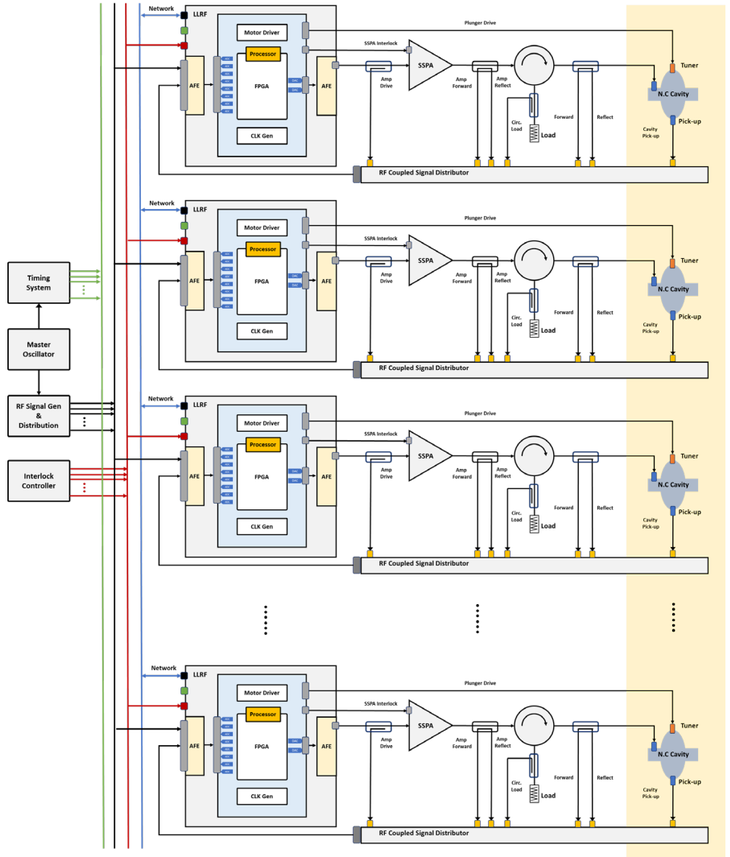




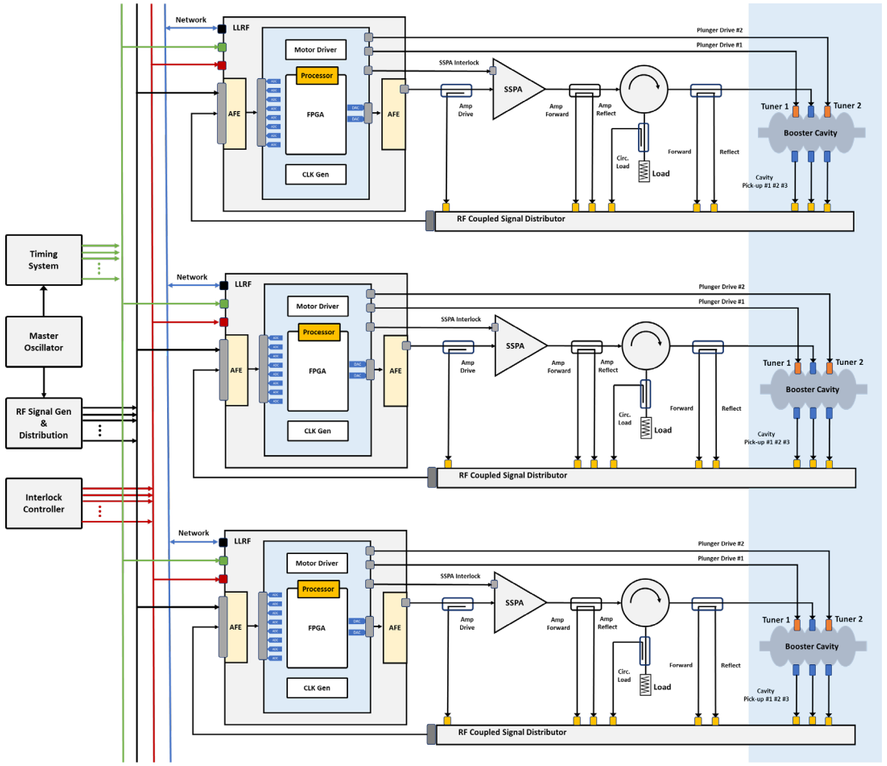
- Storage ring has total 10 of EU-HOM damped cavities.
- Booster ring has total 3 Petra- IV 5cell cavities
- Total 4 straight sections will be required for 10 main cavities and 3 booster cavities.
- To place RF devices, including booster cavities, in one RF building, three booster cavities were placed adjacent to the storage ring cavities.

Overview of LLRF system

- Each cavity is supplied by each SSPA and it is controlled by each LLRF system (individual control)
- Traditional down/up conversion scheme is selected (IF : 50 MHz)
- Share the same hardware platform and common application firmware



Schematic diagram of RF system for storage ring



Schematic diagram of RF system for booster ring

Requirements for stability

- The general expectation is that the amplitude of beam jitters should be less than 10 % of the bunch length

$$\phi_b = \frac{2\pi f_0 L_b}{c}$$

L_b: beam bunch length

f_0 : RF cavity frequency

c : light speed

Parameter		Value
RF frequency [MHz]	f	499.593469
Bunch length [m]	L_b	0.004079
Light speed	c	299792458
Phase tolerance	radian	0.004
	deg.	**0.244**

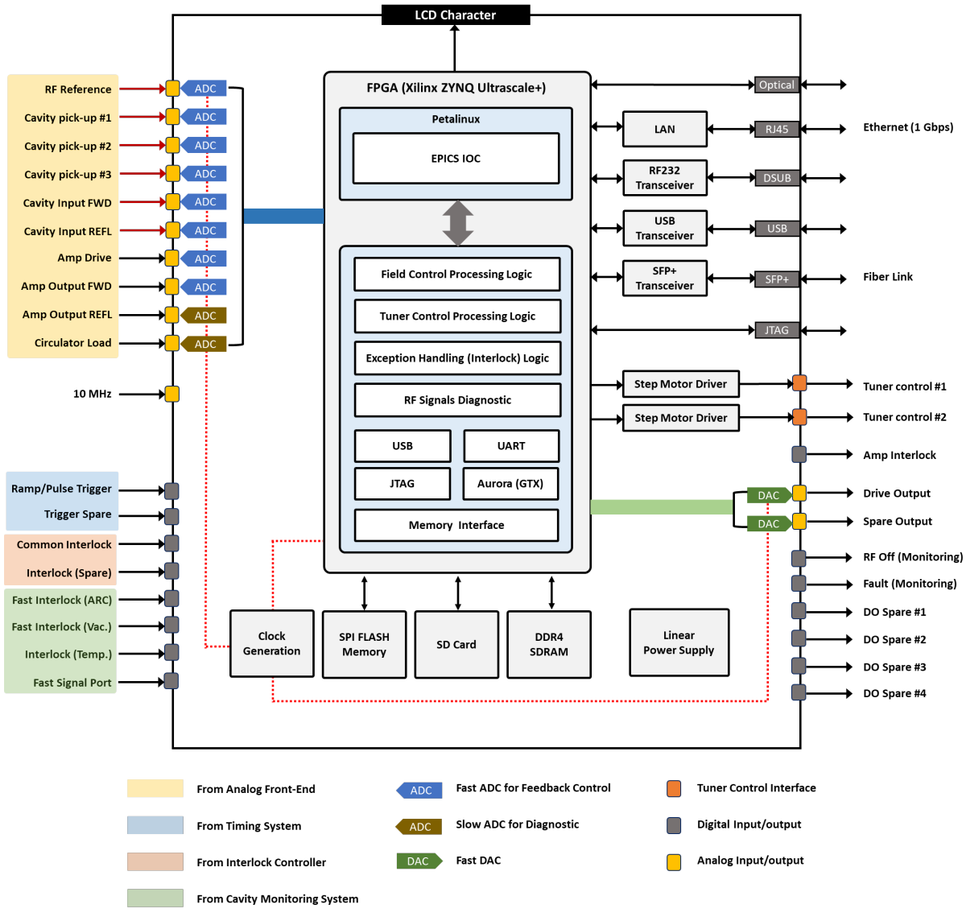
$$\frac{\Delta V_c}{V_c} = \frac{\sin\phi}{\cos\phi}\Delta\phi$$

ø : Synchronous phase

Parameter		Value
Amplitude tolerance	%	**0.271**

- The performance targets of the LLRF system for RF amplitude and phase are within 0.1% and 0.1 °, respectively
- To keep the phase stability less than 0.244° and the RF voltage tolerance less than 0.27%.

Low Level RF system hardware design



Configuration of prototype digital board

Primary specifications of LLRF

Classification	Parameter	Value
General specification	Operating frequency	500 MHz ± 1 MHz
	FPGA chip	Xilinx Zynq ultrascale+
	External trigger	2 inputs, rising/falling edge
RF Inputs	Number of channels	8 (fast) / 2 (slow)
	Channel-to-channel isolation	> 65 dB
	Full scale input level	10 dBm
	Spurious-free dynamic range	> 65 dB
	IF frequency	50 MHz
	LO frequency	450 MHz
	Fast ADC clock	40 MHz (250 MSPS max.)
	Amplitude dynamic range	≥ 25 dB
	Amplitude resolution	< 0.01%
	Amplitude stability	< 0.1 % (upper 10 dB range)
	Phase resolution	< 0.01°
	Phase stability	< 0.1° (upper 10 dB range)
RF outputs	Output channel No.	2
	Full scale drive	10 dBm Max.
Feedback processing	Direct loop delay	< 1000 ns
	Control scheme	CW / Pulse / Ramping
Interlocks	Number of digital input	> 20
	Number of digital output	> 20

Digital component selection and specifications

tentative

❖ ADC (AD9653)

- Resolution : 16 bits
- Sample rate : 125 MSPS
- SNR : 76.5 dB $SNR = 10\log_{10}(P_S/P_N)$
- Latency : 100 ns (estimated)
- Aperture jitter : 135 fs
- Total jitter : 476 fs
- External clock jitter should be less than 456 fs

❖ DAC (AD9783)

- Resolution : 16 bits
- Sample rate : 500 MSPS
- SPURIOUS FREE DYNAMIC RANGE (SFDR) : 68 dBc

$SFDR = 10\log_{10}(P_S/P_H)$

❖ Clock generation (LMK04828)

- Clock jitter < 90 fs

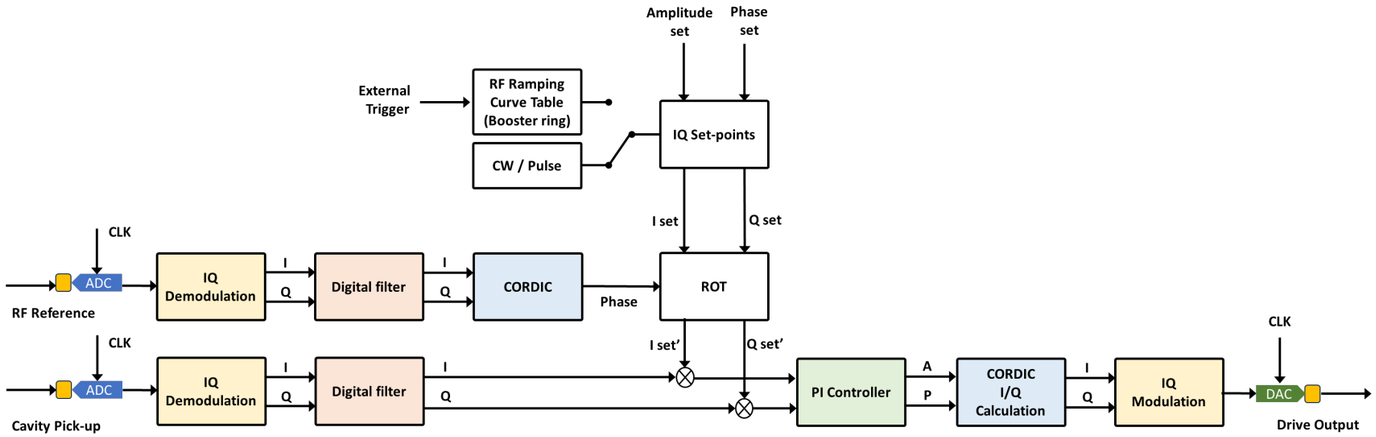
❖ FPGA (ZU9EG)

Zynq® UltraScale+™ MPSoCs: EG Devices

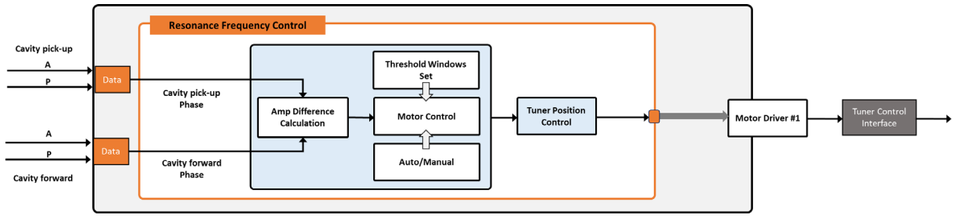
	Device Name[1]	ZU1EG	ZU2EG	ZU3EG	ZU3TEG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.5GHz											
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB											
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5F MPCore™ up to 600MHz											
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core											
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz											
		Memory	L2 Cache 64KB											
	External Memory	Dynamic Memory Interface	x16: DDR4 w/o ECC; x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC											
		Static Memory Interfaces	NAND, 2x Quad-SPI											
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet											
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO											
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains											
		Security	RSA, AES, and SHA											
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor											
PS to PL Interface			12 x 32/64/128b AXI Ports											
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	81	103	154	157	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	74	94	141	144	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	37	47	71	72	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.0	1.2	1.8	2.1	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	3.8	5.3	7.6	5.1	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
		UltraRAM (Mb)	-	-	-	14.0	13.5	18.0	-	27.0	-	22.5	31.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	3	1	4	4	4	8	4	8	4	11	11
	Integrated IP	DSP Slices	216	240	360	576	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
		PCI Express®	-	-	-	1x Gen3x8	2x Gen3x8[2]	2x Gen3x8[2]	-	1x Gen3x16 & 1x Gen3x8[3]	-	2x Gen3x16 & 2x Gen3x8[3]	-	3x Gen3x16 & 1x Gen3x8[3]	3x Gen3x16 & 2x Gen3x8[3]
		150G Interlaken	-	-	-	-	-	-	-	-	-	1	-	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	-	-	2	-	2	4
		AMS - System Monitor	1	1	1	2	1	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	-	8	16	16	24	24	24	32	24	44	44
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	-	-	16	-	28	28
	Speed Grades	Extended[4]	-1 -2 -2L				-1 -2 -2L -3					-1 -2 -2L -3			
		Industrial	-1 -1L -2												

Firmware of LLRF system

- The LLRF system use common digital signal processing method (IQ sampling, digital filter, CORDIC and PI control)
- The control mode of LLRF is divided into Pulse, CW, ramping mode
- The detune angle is calculated by calculating the phase difference between the forward and pick-up signals, and when the detune angle becomes larger than the set control range, the tuner operates so that it can resonate within the tolerance range.



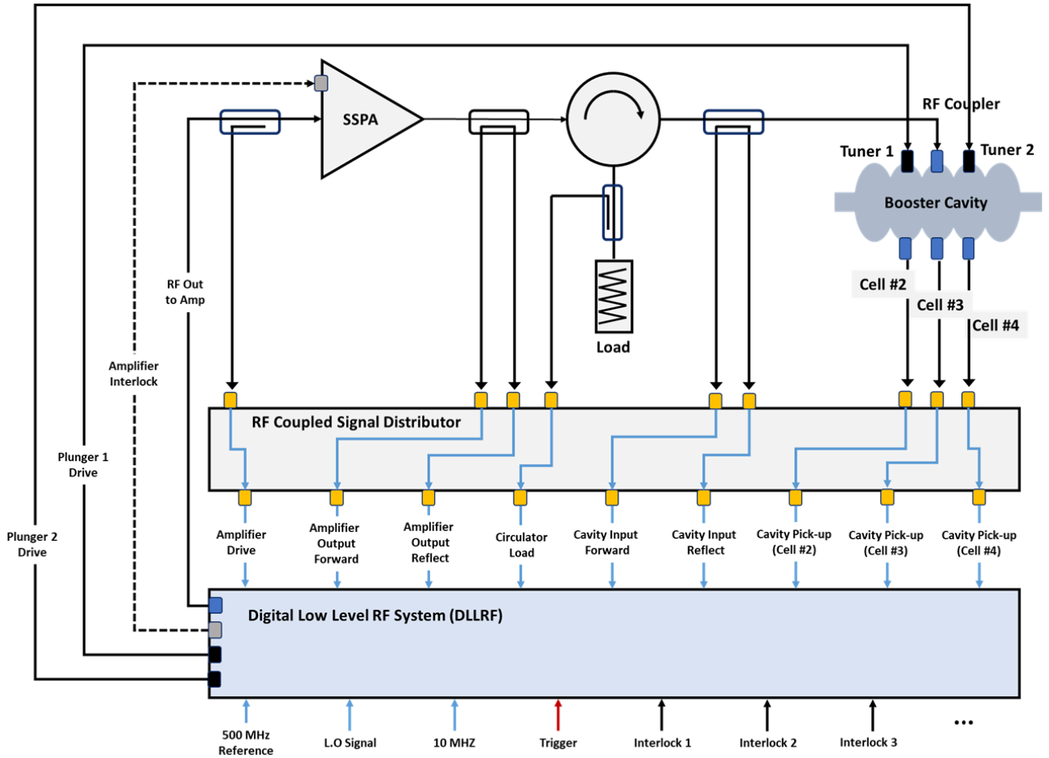
Digital feedback control for amplitude/phase control loop



Digital feedback control for tuning loop

Tuning & Flatness loop for booster ring cavity

- It requires flatness control loop to keep the balance of the electric field distribution inside each cavity cell
- Petra 5 cell cavity has two plunger at cell 2 and cell 4 and three pick-up port for frequency tuning and field flatness control
- Tuning control and flatness control are accomplished by control the plunger positions



RF signal layout for booster ring cavity control

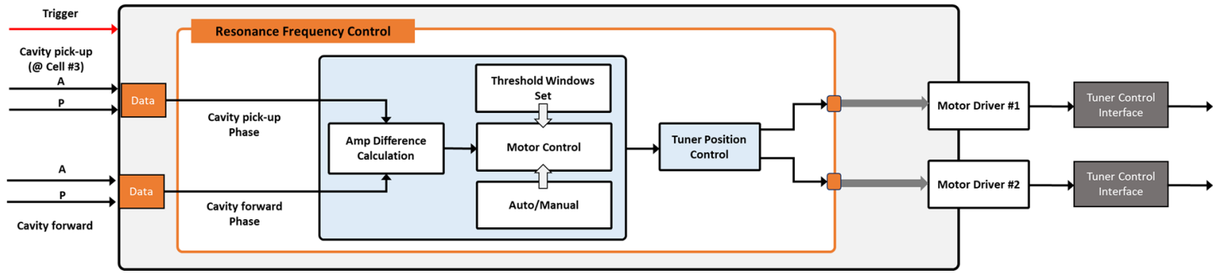
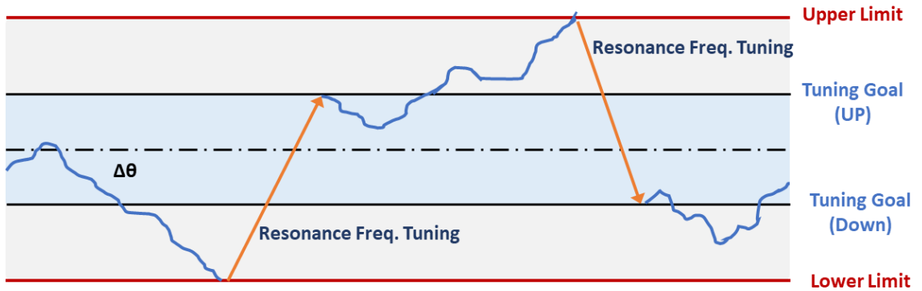


Diagram for tuning loop control



Tuning control scheme

Flatness control loop for booster ring cavity

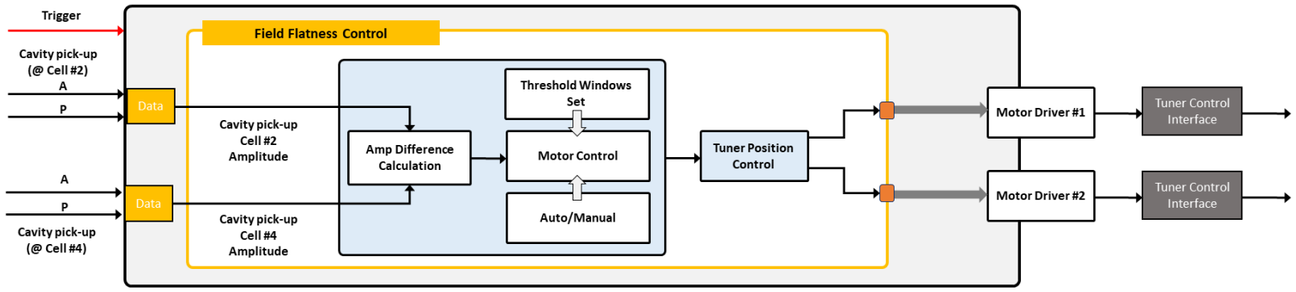
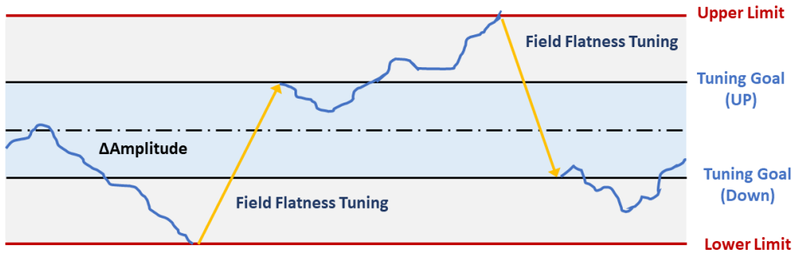
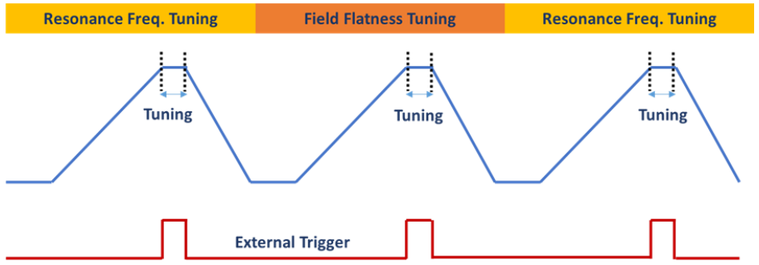


Diagram for field flatness control



Field flatness control scheme

- Two plunger move to opposite direction
- The tuning loop and field flatness loop control are only active when the RF acceleration voltage is in top-up mode
- The tuning loop control and field flatness control loops are synchronized to an external trigger and performed alternately



Process of tuning control and flatness control

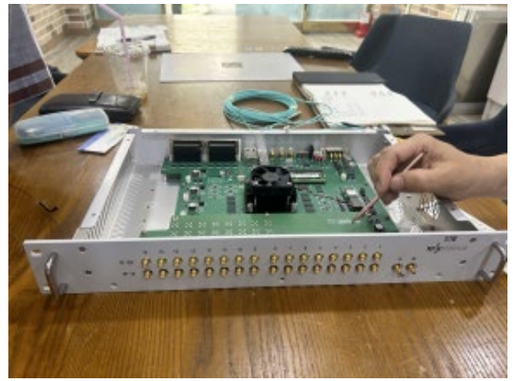
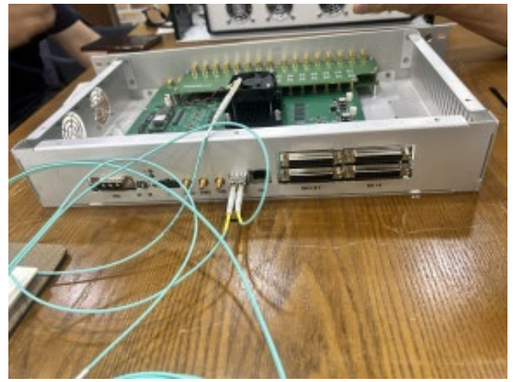
Exhibition booth : Neolinx

Future plan for prototype of LLRF system


2856 MHz LLRF system for PLS-II LINAC



81.25 MHz LLRF system for RAON

Digital system based on RF SOC
for astronomy applications

Exhibition booth : Rohde&Schwarz

Exhibition booth : Instrumentation Technologies

Master oscillator and Distribution system

- Master oscillator (R&S SMA100B)

- Distribution amplifier (Libera DA)
  : supporting also generation of higher harmonics of the RF signal

- Low drift and jitter optical RF signal transfer systems (Libera SYNC) for delivering the signal

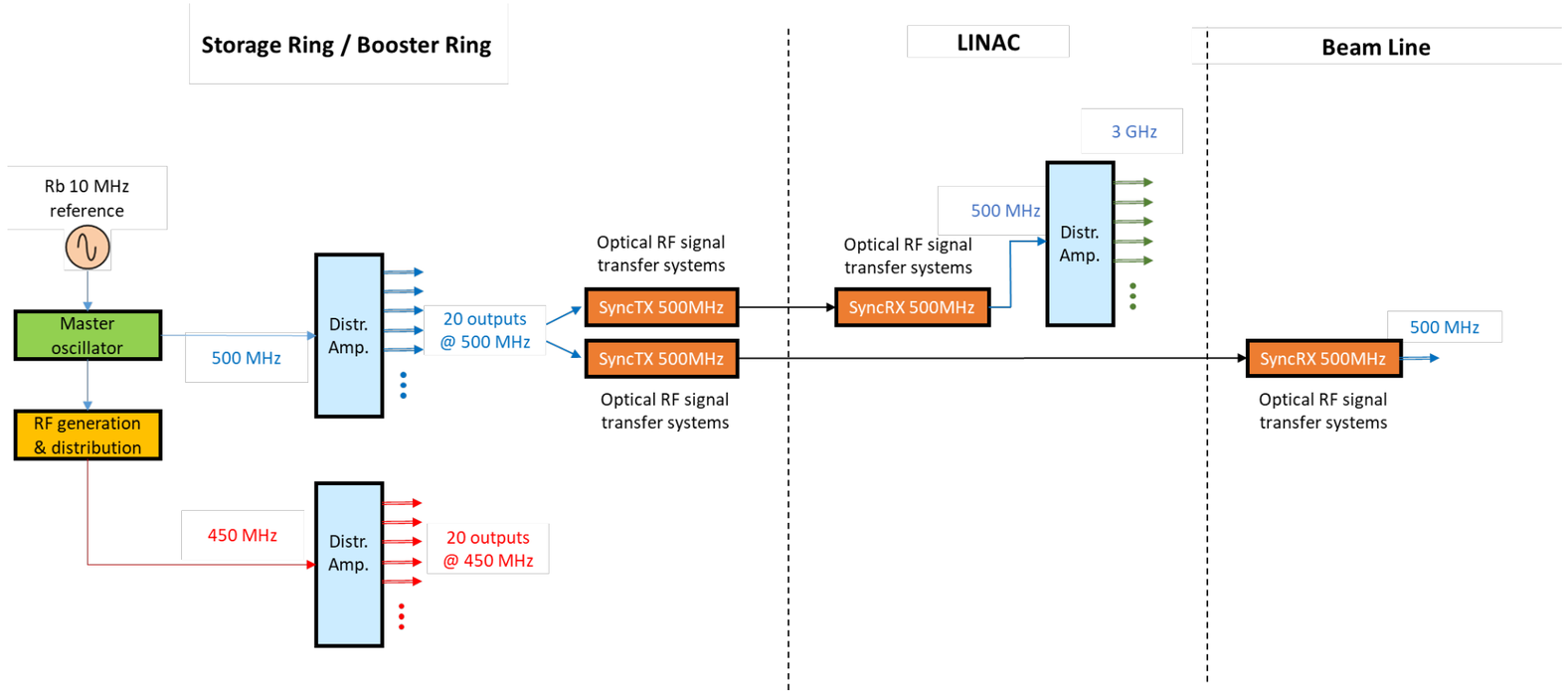


Diagram of RF signals distribution

Thank you for your attention!

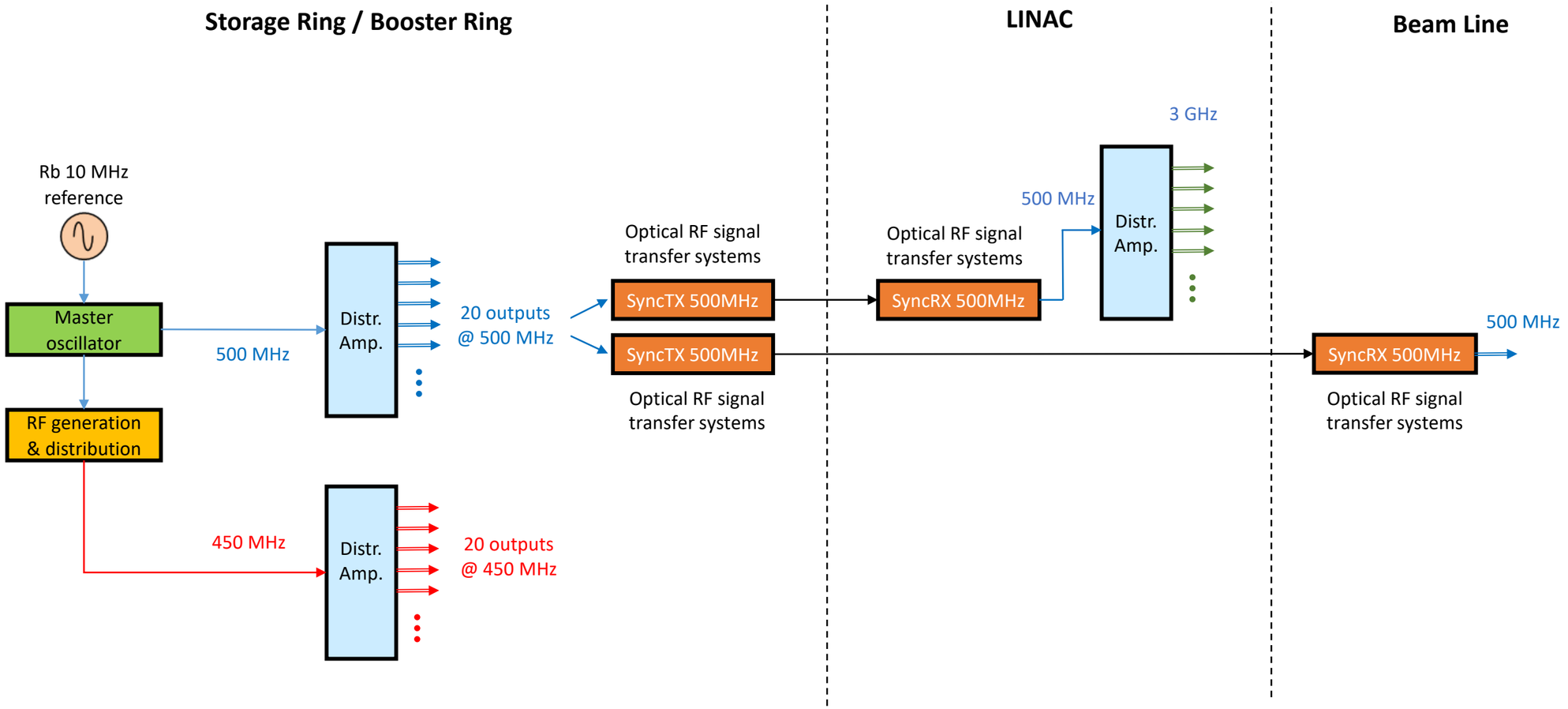
High power RF system

	Number of cavity	8	10	12
Cavity	Required power to coupler [kW/unit] (case of single cavity failure)	127.07 (145.22)	**98.57** **(109.52)**	80.73 (88.07)
Transmission	Reflect power [kW/unit]	0.042	**0.448**	0.629
	Transmission line loss (Pt/unit)	10	**10**	10
SSPA	Output power of HPRF [kW/unit] (Case of single cavity failure)	137.07 (156.65)	**108.57** **(120.66)**	90.73 (98.98)
	Rated power of SSPA [kW/unit]	190	**150**	130

Exhibition booth : Rohde&Schwarz

Exhibition booth : Instrumentation Technologies

Storage ring RF cavity



Concept diagram of the 150 kW SSPA

Master oscillator and Distribution system

- Master oscillator (R&S SMA100B)

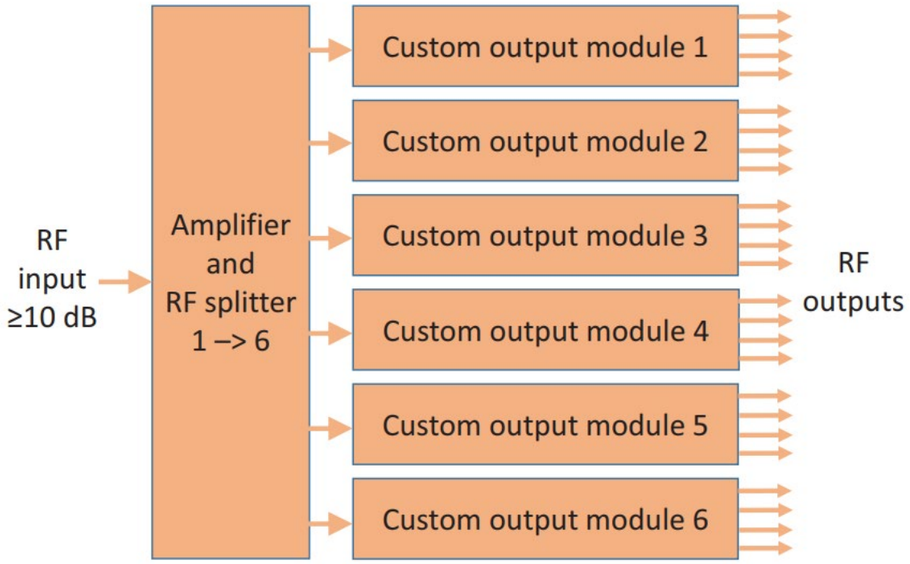
RF output:

- 500±1 MHz will be used in 4GSR
- from 8 kHz MHz to 3 GHz
- remotely configurable
- 15 dBm, 50 Ω
- integrated phase noise (jitter) from 10 kHz to 5 MHz: <18.7 fs RMS

Ethernet interface, EPICS IOC available

Master oscillator and Distribution system

- Distribution amplifier (Libera DA)



- It can be customized in terms of number of RF outputs
- The freq. of the outputs can be divided or multiplied from the provided input freq.

RF input:
- 500 MHz
- 15 dBm

RF outputs:
- Modular arhitecture supports up to 24 RF outputs at different harmonics of the input frequency:
  x1 : 500 MHz (for Booster, Storagerig, Timing system,...)
  x6 : 3000 MHz (for LINAC)
- Other multiplication and/or division factors are also possible.
- 15-18 dBm

Integrated added jitted from 10 Hz to 10 MHz: <5 fs RMS

Master oscillator and Distribution system

- Low drift and jitter optical RF signal transfer systems (Libera SYNC)

Features

- RF reference signal that modulates an optical carrier through an electro-optical modulator. The modulated signal is fed into the optical links

- At the receiver, the optical signals are demodulated into the RF domain. The low-jitter signal is amplified, filtered, and stabilized in amplitude and phase

- This signal is used to provide two RF outputs and one monitoring output

RF input

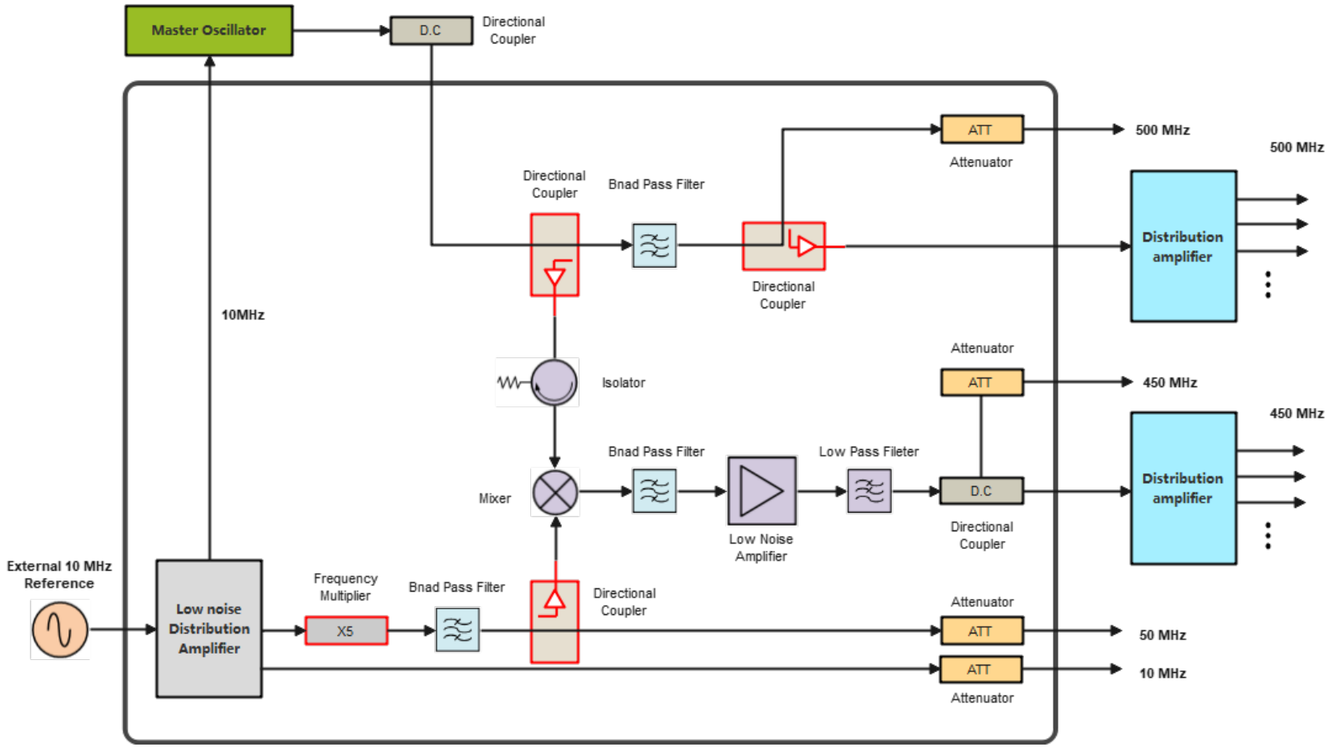
- 500 MHz
- 15 dBm

RF outputs

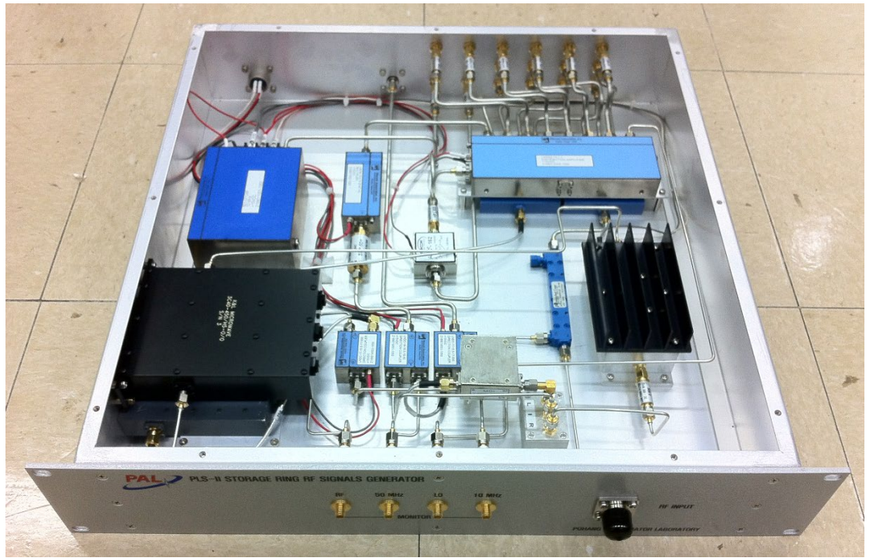
- 15-18 dBm
- Integrated added jitted from 10 Hz to 10 MHz : <300 fs RMS
- Maximal optical link length : 1500 m

RF and LO generation chassis

- 1st stage : 3 of 10 way cavity combiner (tested RL 42 dB)
- 2nd stage : 1 of 3 way WR1800 WG combiner(tested RL 39 dB)
- Final stage : Prototype 150kW SSPA package



Concept diagram of the 150 kW SSPA



Concept diagram of the 150 kW SSPA